# Design & Implementation of Digital to Digital Converter Comprising Ternary Logic to Binary Logic

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**Abstract:**

The structural design & realization of ternary TRIT to binary BIT converter is described. The objective of this converter is to suggest the ENSUING compatibility ISSUES between ternary & binary systems. The proposed ternary to binary converter is IS MEANT to convert 4 trits of ternary logic into 5 bits of binary logic HOWEVER; BE EXTENDED TO DESIRED NUMBER OF TRITS. Aforesaid ternary to binary converter provides an easy method for inter conversion from ternary to binary logic. Ternary TRIT signals are used as an input TO THE PROPOSED converter TO BE CONVERTED TO BINARY BITS using CMOS DEVICES. Binary logic gates are used for switching of MOSFET matrix. The design is implemented using cadence schematic editor and simulated using cadence virtuoso analog design environment at 180nm CMOS process technology.

Index Terms: Binary, Converter, CMOS, MVL, NMOS, PMOS, Ternary, TRITS

## 1. Introduction:

Ternary logic is one of the emerging fields in digital electronics. Levels 0, 1, 2 represent low, intermediate & high voltage levels. The current systems work on binary logic. Ternary logic has 3 levels which provide many advantages over existing binary system including HIGHER DATA PER TRIT, reduced interconnection required for implementation of logic AND WHERE . Applications need higher speed of operation, Ternary logic is proved to be an MOST OPTIMUM DIGITAL SYATEM option [1] [2] [3]. The system having higher radix than 2 shows faster speed of calculation in arithmetic operation as smaller number of digits is required. The channel capacity can be utilized effectively as higher information content can be transmitted. To have compatibility BETWEEN binary & ternary logic system, a ternary to binary converter can be used.

## 2. Ternary Decoder:

The ternary decoder [4] is composed of three different ternary switches. Here padding of two MOS transistor is used. This decoder is composed of total 10 transistors. Threshold voltage of switches is adjusted by padding of MOS transistors. By padding of PMOS in switch1, the input falls to low level. On the other hand if NMOS is considered the input is raised to high level. The desired ternary logic level is obtained by changing the threshold of a transistor.

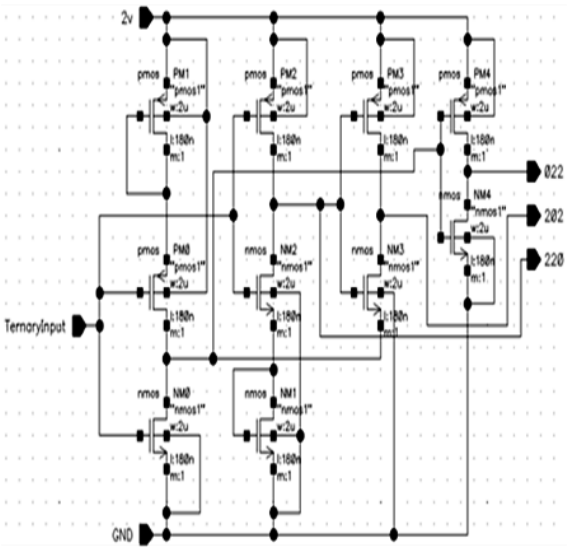


Fig1: Ternary Decoder

3. Ternary to Binary Converter:

Ternary to Binary converter is shown in fig.1. Ternary decoder gives two level output. This output of ternary decoder is used to switch the MOSFET matrix to obtained desired output. For this purpose the standard decoder circuit is used. The decoder circuit consists of NOR gate & an inverter. As the ternary input is applied to the decoder, corresponding gate will become on & desired MOSFET matrix gives the binary output. As shown in figure 2 the decoder circuit uses ternary input. Output of decoder has two levels 0 & 2. These outputs are applied to the ternary to binary converter which drives the matrix of MOSFET producing desired output.

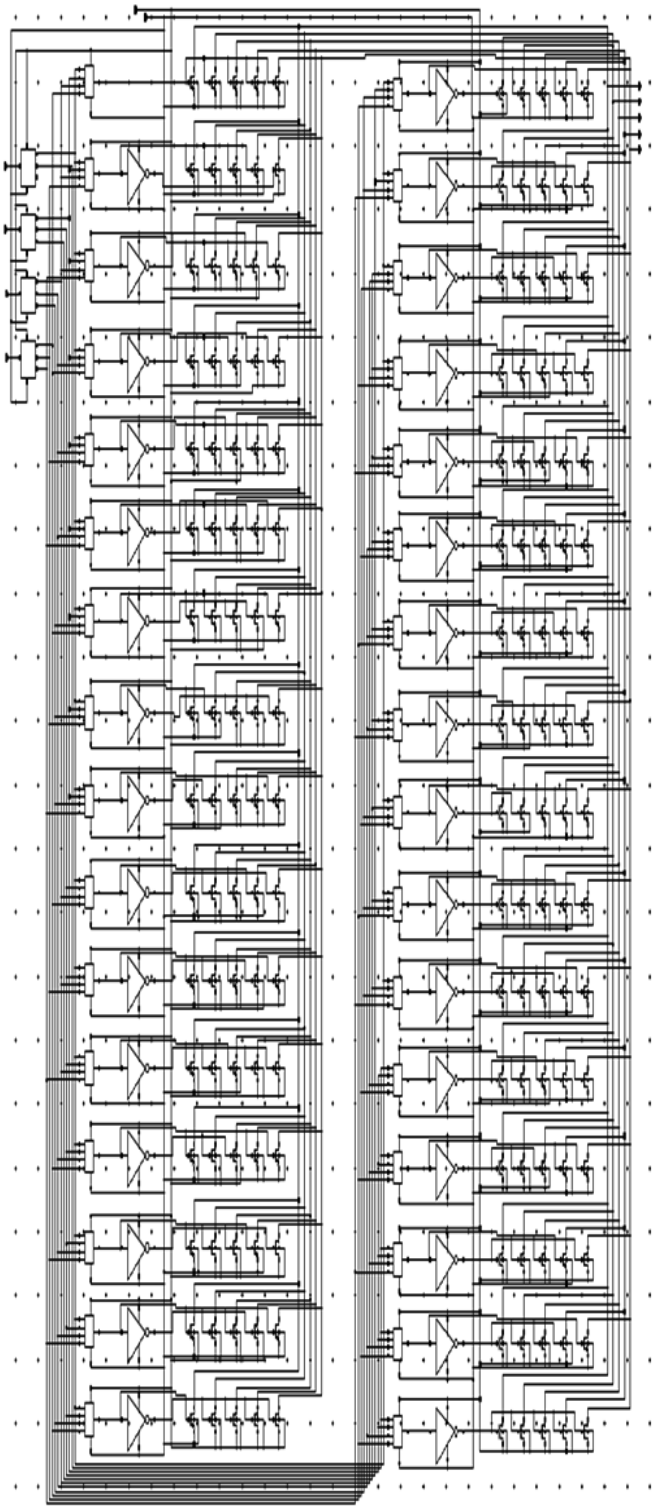

Fig.2: Ternary to Binary Converter

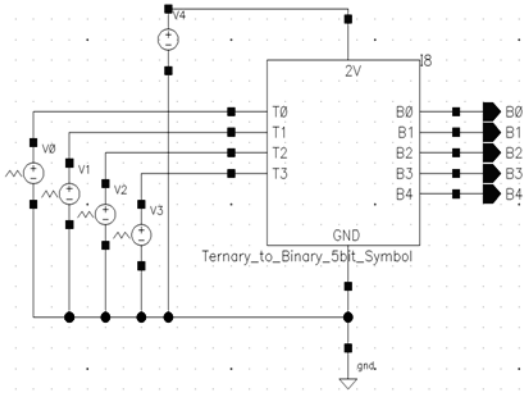


Fig3: Block Diagram of Ternary to Binary Converter

4. Simulation Results:

Here the implementation of proposed ternary to binary converter is illustrated. Cadence schematic editor and Cadence virtuoso analog design environment is used for simulation. The transient responses of above designs are shown in figure 4. Ternary logic levels of 0, 1 & 2 Volts are applied in the input. In output, binary 0 & 2 Volts are obtained.

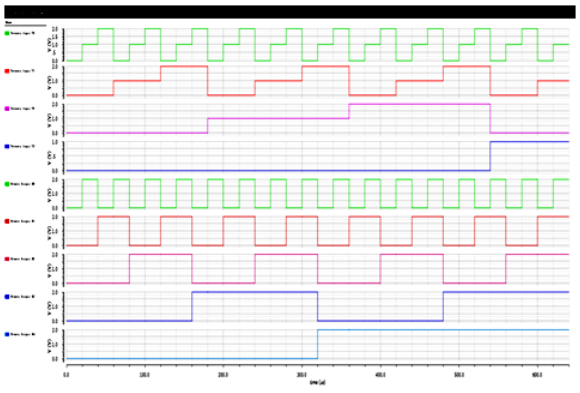

Fig 4: Ternary to Binary Converter Input & Output Waveforms

5. Conclusion:

The proposed Ternary to Binary converter is designed & simulated successfully. Ternary input is applied to the converter & desired binary output is obtained. Hence this design is useful in bridging the gap of compatibility between ternary & binary systems. Also conversion time is COMPARABLEl & desired output BIT voltages are obtained.

References:

1) D.I.porat "Three valued digital system" Proc.IEE Vol.116, No6, P.947-955, June 1969.

2) K.C.Smith "The prospects of multivalued logic technology & application view" IEEE transaction on computer, Vol.-C -30, P-619-627 September 1981.

3) P.C.Balla & A.Antoniou "low power dissipation MOS ternary logic family" IEEE journal on solid state circuits Vol. Sc-19 no-5, P.739-749, October 1984.

4) Optimization Of Cmos Devices In Multi-Valued Logic Decoder International Journal of Scientific & Engineering Research ISSN 2229-5518

5) H.T.Mouhtaf & I.B.Jordan “Study on the implementation of three valued logic". Proc.ISMVL, P.359-372 May 1975.

6) Seiichi Muta "Micropower CMOS implementation of three valued logic function". Proc.ISMVL, P 61-63, May 1983.

7) Michel Israel & D.Etiemble “Some new results for ternary circuits"". Proc.ISMVL, P 66-69, May 1979.

8) Chung-Yu-Wu"Design & application of pipelined dynamic CMOS ternary logic & simple ternary differential logic" IEEE journal on solid state circuits Vol.28, No-8, August 1993.

9) T.Higuchi & M.Kameyama "Synthesis of optimal T-gate networks in multiple valued logic" Proc.ISMVL, P.190-195, May 1979.

10) G.Rosenfeld & M.Yeoli "Logical on electronic computers.P.19-29, V0l.EC-14 February 1965.

11) E.Mccluskey"Logic design of MOS ternary logic"Proc.ISMVL,P.1-5,May 1980.

12) T.C.Yang" A minimization algorithm for ternary switching functions "Proc. ISMVL P.241-253, May 1975.

13) J.Huertas & J.Carmona "Low power ternary CMOS circuits. Proc.ISMVL P.170-174, May 1979.

14) T.Sasao “Compact SOP representation for multiple output functions-An encoding method using multiple valued logic” Proc.ISMVL 2001.

15) I.Halpern & M.Yoeli “Ternary arithmetic unit” Proc.IEE, Vol.115,No.10,pp. 1385-1387, Oct. 1968

16) D.Hamilton & W.Howard "Basic Integrated Circuits Engineering"McGrawHill, Motorola series in solid state electronics.

17) R.P.Hallworth & F.G.Heath “Semiconductor circuits for ternary logic” The institution of electrical engineers, Monograph No.482E Nov.1961, p.p.219-223.

18) T.Hanyu, M.kemayama,C.Zukeran “Multiple-valued mask programmable logic array using one-transistor universal literal circuits. Proc.ISMVL 2001.