Design Of 3-Valued R-S & D Flip - Flops Based on Simple Ternary Gates

A.P.Dhande and V.T.Ingole

***Abstract*—** Design of 3-valued R-S & D type of flip-flops is described. A new clock is developed according to which circuit makes transition as well as retains present, past & former past information. The proposed flip-flops are constructed using clocked T-Gates that reduces the number of transistors required to implement single clocked gates. In the verification by simulation, the proposed flip-flops appear to have lesser power consumption, better speed of operation.

***Keywords*—** Ternary, Flip-Flops, T-gates.

I. Introduction

Ternary means a switching element, which switches between 3 levels, such levels denoted bye x may assume either x^0,x^1,x^2 where 0,1,2 signifies logic levels (voltage levels) as 0,1,2. Ternary system has several important advantages over binary. It can be summarized as reductions in the interconnections require to implement logic functions, thereby reducing chip area, more information can be transmitted over a given set of lines, lesser memory requirement for a given data length. Besides this serial & some serial-parallel operations can be carried out at higher speed Its advantages have been confirmed in the application like memories, communications and digital signal processing etc. [1][2][3].

Recent articles have shown much interest in the design of ternary memory circuits [4],[5],[6],[7],[8][9].Many approaches and different realization schemes have been suggested .The excitation equation of binary D, T, RS, JK are used in the design of ternary flip-flops. The description of 3- valued memory elements is found in the references [10], [11].

In present work, it is suggested that flip-flops based on new ternary clocked gates reduces number of T- gates as compared with the clocked T-gates proposed in [3],[12],[13].

An organization of this paper is as: section II describes basic clocked T- Gates. Section III design & working of R-S, D type of flip-flops is given. Section IV discusses an application of D FF to ternary encoder, In Section V Comparison with other circuits is made & finally conclusion & references are given in section VI & VII respectively

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II. TERNARY LOGIC GATES.

The most fundamental building blocks in the design of digital system are INVERTERS, NOR & NAND gates. The basic ternary inverters namely simple ternary inverter (STI), positive ternary inverters (PTI) & negative ternary inverters (NTI) forms an operator set that is complete in logic sense. All these inverters are combines to realize the logic functions like T-AND/T-NAND, T-OR/T-NOR etc.

In general, ternary inverters, AND & OR functions are defined as:

$$\text{STI} = \overline{x}^{i} = 2 - x$$

$$\text{PTI \& NTI} = \overline{x}^{i} = i \text{ if } x = i$$
$$= 2 - i \text{ if } x \neq i \text{ where } i \text{ can be 2 or 0}$$

$$\text{TOR} = \text{Max}(x, y) \;\&\; \text{TAND} = \text{Min}(x, y)$$

Table 1 show truth table for STI, PTI & NTI.Logic symbols for STI, PTI, & NTI is given in Fig.1 (a) & implementation of STI, NTI &PTI is given in Fig.1 (b).

Table 1 Truth

Input X	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

(a)

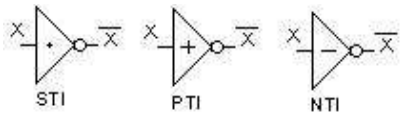

Fig. 1 (a)

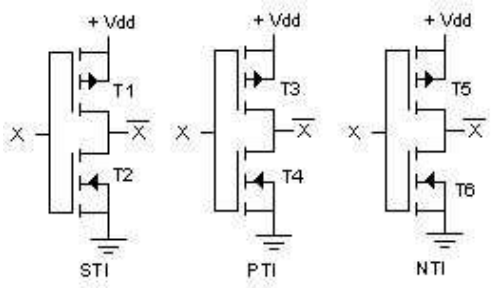

Fig.1 (b)

Fig.1 (a): Logic symbols for STI, PTI, & NTI
Fig.1 (b): Implementation of STI, PTI & NTI

Fig.2 shows the implementation of STNAND & STNOR.In the implementation of these gates T1, T2 are P-channel enhancement & T3, T4 are N-Channel enhancement transistors with the device parameters as in Table 2. The logic level defined in proposed gates are 0=0v, 1=2.5v. & 2=5v

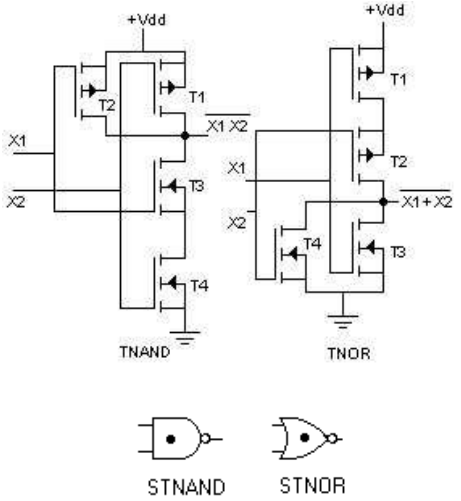

Fig.2 Implementation of STNAND & STNOR

TABLE: 2 DEVICE PARAMETERS

	T1 & T2	T3 & T4
Device type	P-channel enhancement	N-channel enhancement
Threshold voltage	-0.4588 v	0 v
Drain ohmic resistance	1M	1M
Surface potential	0.6v	0.6 v
Bukl junction saturation current	1e-14 A	1e14 A

In the operation of this circuit, when Vi=2.5 V (Logic level 1), T1 & T2 both are ON since V_{gs1} & $V_{gs2} > V_{T,\ So}$ the static power consumption is given as :

$$P = Vcc^2 \times \left(\frac{R1\ R2}{R1 + R2}\right)$$

$$\left(\frac{R1\ R2}{R1 + R2}\right) = R$$

$$P = \frac{Vcc^2}{R}$$

Since, denominator value is very large; the static power dissipation is very small.

The output of clocked NAND gate is shown fig. 3 Here X1 is connected to 5 v (Logic 2) & X2is connected to clock. Truth tables for all standard gates are given in ref. [14].

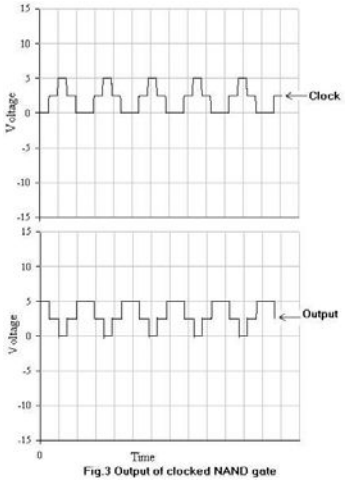

Fig.3 Output of clocked NAND gate

III. DESIGN & WORKING OF R-S FLIP-FLOP.

As a way to compose ternary flip-flop, the similar structure of flip-flops as in binary is applied. The fundamental flip-flops in binary logic are designed using NAND/NOR binary gates. Therefore by replacing binary gates by ternary gates it is possible to construct ternary flip-flops. Fig.4 shows structure of R-S flip-flop and its truth-table is given in table 3.

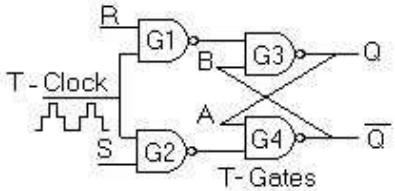

Fig.4 Structure of R-S flip-flop

TABLE .3 TRUTH TABLE FOR R-S FLIP-FLOP

Clock	S	R	Q	$\overline{Q}$
0	0	0	0	2
0	0	1	0	2
0	0	2	0	2
1	1	0	1	1
1	1	1	1	1
1	1	2	1	1
2	2	0	2	0
2	2	1	2	0
2	2	2	2	0

Assuming initially clock =0,R=2,S=0 & Q=0,here output of G1 is 2 & G2 is 0. Output of G4 will be 2whish is applied to G3, so the output of G3=0.Thus Q & Q are complimentary to each other. The truth table can be verified for clock=0,1,2 with different logic levels of R & S.

The performance of the flip-flop is verified using Electronic Workbench Version 5.0. Fig.5 (a) shows output waveform synchronized with ternary clock with inputs S=0&R=2 &(b) when S=R=1.The operating speed of flip-flop depends upon switching speed of T-gates.With the proposed T-gates operating speed is 100ms however it can be improved by adjusting the parameter, peak current density of the devices, by decreasing parasitic R-C components. The parametric value for T-gates in the proposed circuit is Peak current density = $1x10^3 A/cm^2$.

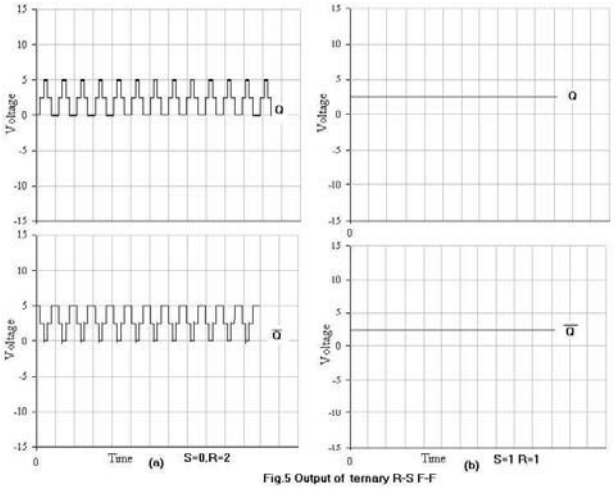

Fig.5 Output of ternary R-S F-F

On the basis of R-S Flip-Flop, clock synchronized D-type flip-flop is constructed. The circuit for D-latch is shown in Fig. 6. It has only one input refereed to as D input .Its truth table is given in Table4 form which it is clear that output Q_{n+1} at the end of clock pulse equals to input D_n before the clock pulse.

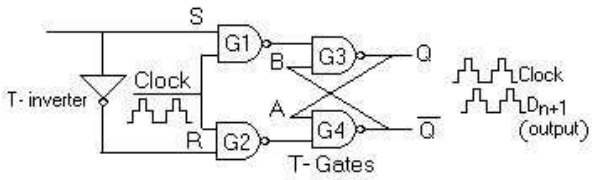

Fig.6 D-Latch

TABLE 4. TRUTHTABLE FOR D-FF

Input Dn	Output Dn+1
0	0
1	1
2	2

IV. APPLICATION OF D-FF TO ENCODER FOR TERNARY CODE

As an application of D-FF we consider its application to ternary encoder. As a means of data communication, ternary codes are preferred because of its information carrying capacity is much higher than binary. Assume, message block as 11201(=k) in ternary code. The encoder generates message block of size n (k < n). Fig.7 shows ternary encoder.

Here D1, D2 &D3 are ternary flip-flops. For the generation of codes assume all the flip-flops are cleared initially. During message bit interval commutator samples the modulo-3 adder outputs c_1, c_2 c_3 which is given by the equation.

$$C_1 = D1 \oplus D2 \oplus D3$$
$$C_2 = D1$$
$$C_3 = D1 \oplus D2$$

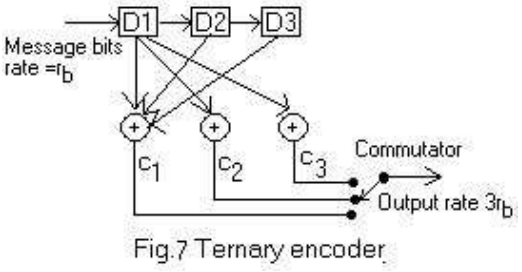

Fig.7 Ternary encoder

Thus single message bit gives three output bits. The next message bit in the input sequence enters the D1 and contents of D1are shifted to D2.Commutator again samples the output during next bit interval. The process is repeated untill last digit shifted to D3. The sequence of code generated by encoder is shown in fig.8

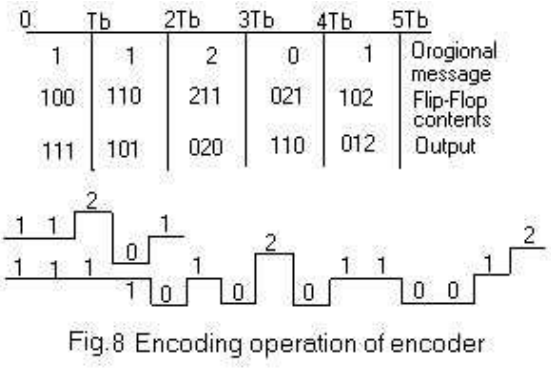

Fig.8 Encoding operation of encoder

V. COMPARISON WITH OTHER CIRCUITS

The main advantage of our T-gates is fewer number of FET required compared to other T-gates. To design single clocked NAND/NOR gate, number of FET required in our case is 4 where as in ref.[3][12] is 7 & 6 respectively.

The operating speed of T-gates in our case is 100ms where as same in ref.[3] [12] is 20 ns &150 ns.

In ternary logic, noise margin is defined as NM_0, NM_1, NM_2 & NM3. It depends upon design of gates i.e. gate with duel supply voltage or single supply voltage. In our case with supply voltage =5v, NM0 = NM_1= NM_2 = NM3 .75v. Proposed gates can be operated at 3.3v but it is very difficult to get high noise margin.

We are using ternary clock rather than binary .The main problem of binary clock is it requires its simple & inverted form for the operation of circuit [12],which is avoided using ternary clock.

VI. CONCLUSION

The R-S & D flip-flops based on new ternary gate is described. These gates required lesser number of FETS than compared one. In the verification through simulation, proposed flip-flops have fair results like less power consumption, speed of operation etc.

An application of proposed gates can be extended to any sequential logic circuit in ternary digital system.

VII. REFERENCES

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