Design & Implementation of Digital to Digital Converter comprising Binary Logic to Ternary Logic

Vinay U. Kale Vijay T. Ingole Vikram S. Ingole Ashwin K. Thakur

Abstracts:

The structural design & realization of Binary to Ternary converter is described. The objective of this converter is to suggest a solution for compatibility between emerging ternary & binary systems. The suggested Binary to Ternary converter is implemented using ‘m’ trits of Ternary logic into ‘n’ bits of Binary logic conversion. Aforesaid converter provides a fast method for digital conversion from Binary to Ternary logic. Binary signals are used as an input to the converter for converting in to ternary signals using matrix of MOSFET devices. Binary logic gates are implemented for switching the MOSFET matrix. The design is implemented using cadence schematic editor and simulated using cadence virtuoso analog design environment of 180nm CMOS process technology.

Index Terms: Binary, Ternary, Converter, CMOS, MVL, NMOS, PMOS.

INTRODUCTION:

Ternary logic is one of the emerging fields in digital electronics and computing machines. Most of the current systems work on binary logic. Ternary logic has 3 levels which provide many advantages over existing binary system including reduced interconnection required for implementation of logic. When an application needs higher speed of operation, Ternary logic is proved to be an excellent option [1,2,3]. Unbalance Ternary logic system has 0, 1, 2 representing low, intermediate, & high logic levels [4]. The system having higher radix than 2 shows faster speed of processing in arithmetic operation as less number of digits is required [5,6]. The channel capacity can be utilized more effectively as higher information content can be processed [7], therefore for the compatibility of binary & ternary logic system, a Binary to Ternary converter is essential.

1. PROPOSED BINARY TO TERNARY CONVERTER:

The 3 bit binary input A, B, C is incorporated in binary to ternary converter circuit. The 3 *bit* Binary to 2 *trit* Ternary converter circuit comprises plurality of circuit comprising an inverter, a NOR gate and a transmission gate. Binary input is given to inverters and then given to a NOR gate. Where NOR gate is the remaining half of the Binary to Ternary converter circuit.

The remaining section of the Binary to Ternary converter comprises PMOS, NMOS and a transmission gate. Depending on the ternary output, the combinations of

above gate are implemented to convert the inputs in to corresponding outputs. Thus the circuit converts three binary signals into fraction of two trit ternary signals[8].

For 'n' trit ternary system, total 3^n digital combinations are possible and for 'm' bit binary system, total 2^m digital combinations are possible. Hence,

$$n*\log 3 = m*\log 2$$

$$\frac{m}{n} = 1.58$$

For example an n=32 trit ternary system and a 32 bit binary will have counting ratio $3^{32}/2^{32}$ = 431440. This means 32 digit ternary based systems will process the information 431440 times more than contemporary 32 bit binary computer architecture [9].

1.1 Transmission Gate (TG):

CMOS TG is shown in Figure 1 along with its symbol. It is designed using P of N channel MOSFET. TG allows Vin to be connected to output Vout when enabled while keeps input, output isolated when disabled. Enabled means when $Vg_1 = -V_{DD}$ and $Vg_2 = +V_{DD}$ to make both transistors are on. The input voltage Vin is then connected to output Vout through the parallel ON resistance of the channels formed by two transistors. While disabled means when $Vg_1 = V_{DD}$ and $Vg_2 = -V_{DD}$ switching OFF both transistors. In certain configuration the resistance between Vin and Vout may be of many orders of ohm (10^9Ω) [10,11].

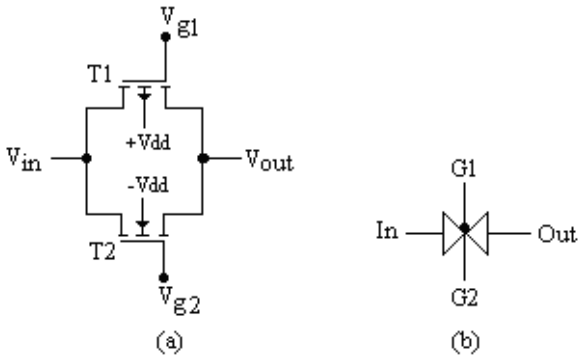

Figure 1(a) Design of Transmission Gate (b) Symbol of Inverter

1.2 Design of Inverter:

A logic gate is an idealized physical device implementing a Boolean function, that is, it performs a logical operation on one or more logic inputs and produces a single logic output. In digital logic, an inverter or NOT gate is a logic gate which implements logical negation. The truth table 1 and symbol is shown in Figure 2. A NOT gate is also called an inverter. The circle on the triangular symbol is called a bubble, and is used in logic diagrams to indicate a logic negation between the external logic state and the internal logic state (1 to 0 or vice the versa). The circuit symbol must be

accompanied by a statement asserting that the positive logic convention or negative logic convention is being used (high voltage level = 1 or high voltage level = 0, respectively) [12].

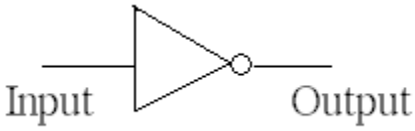

Figure 2: Symbol of NOT gate

Input	Output
1	0
0	1

Truth Table 1: NOT gate

1.3 Design of NOR Gate:

The NOR gate is a digital logic gate that implements logical NOR operation according to the truth table 2. When both the inputs to the gate are LOW (0) a HIGH output (1) results; if any one or both inputs are HIGH (1), a LOW output (0) results. NOR is the result of the negation of the OR operator. NOR is a functionally complete operation, combinations of NOR gates can be combined to generate any other logical function. The Truth Table 2 and symbol of NOR gate shown in Figure 3. By contrast, the OR operator is monotonic as it can only change LOW to HIGH but not vice versa [12].

Figure 3: Symbol of NOR gate

Input $_A$	Input $_B$	Input $_C$	Output $_Y$
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Truth Table 2: NOR gate

2. SCHEMATIC:

2.1 Schematic of Inverter:

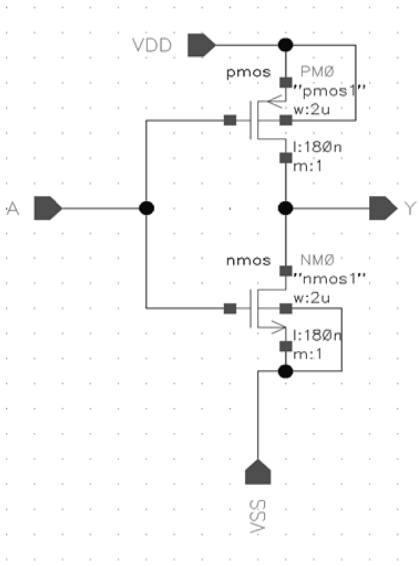

Figure 4: Schematic of Inverter

2.2 Schematic of NOR Gate:

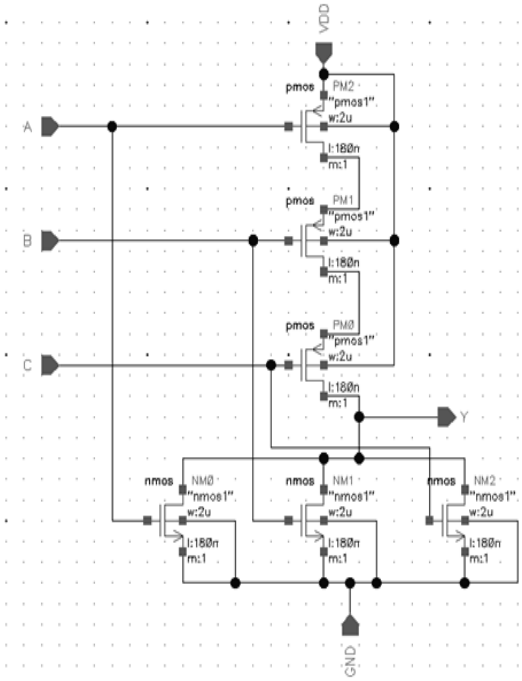

Figure 5: Schematic of NOR Gate

2.3 Schematic of 3bit Binary to Ternary Converter:

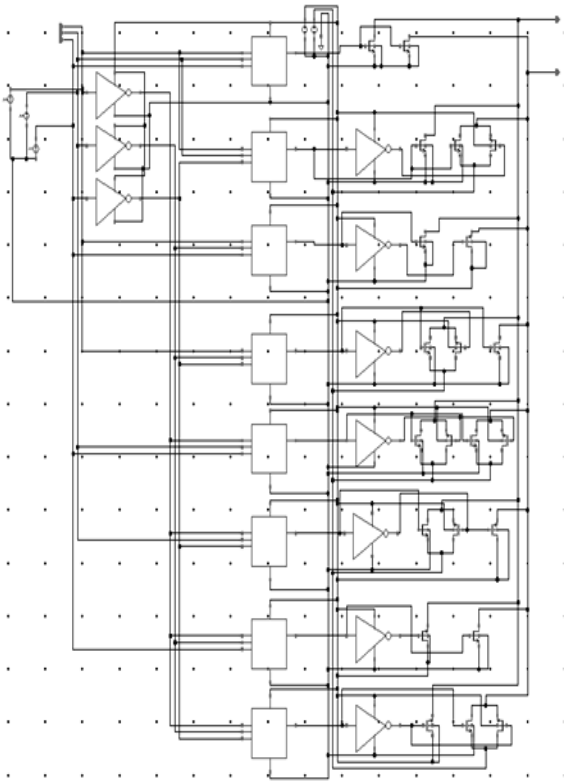

Figure 6: Schematic of Binary to Ternary Converter

3. SIMULATION RESULT:

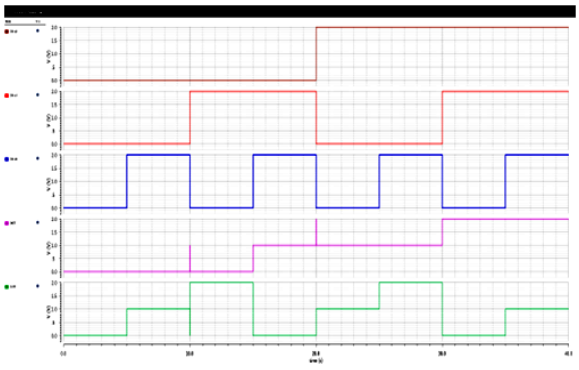

Figure 7: Simulation Result of Binary to Ternary Converter

4. CONCLUSION:

The proposed Binary to Ternary converter circuit is being designed and simulated. Simulation results show the successful implementations of a fast method realized by combination logic circuits for converting Binary signal to Ternary is successfully implemented.

REFERENCES:

[1]Ternary Digital System: Concepts and Applications A. P. DHANDE, V. T. INGOLE, V.R.GHIYE Published by SM Medical Technologies Private Limited Copyright © 2014 SM Medical Technologies Private Limited.

[2] V.U.Kale, V.T.Ingole, V.S.Ingole, Optimization of CMOS Devices in Multi-Valued Logic Decoder International Journal of Scientific & Engineering Research ISSN 2229-5518, NOVEMBER 2016.

[3]A.P.Dhande and V.T.Ingole, Design Of 3-Valued R-S & D Flip – Flops Based on Simple Ternary Gates, World Academy of Science, Engineering and Technology 4 2005.

[4] H.T.Mouhtaf & I.B.Jordan "Study on the implementation of three valued logic". Proc.ISMVL, P.359-372 May 1975.

[5]K.C.Smith,"The prospects of multivalued logic technology & application view" IEEE transaction on computer, Vol.-C -30, P-619-627 September 1981.

[6]A.P.Dhande and V.T.Ingole, "Design of 3-Valued R-S & D Flip – Flops Based on Simple Ternary Gates" World Academy of Science, Engineering and Technology 4 2005.

[7]M. Yoeli and G. Rosenfeld, "Logical Design of Ternary Switching Circuits" Member, IEEE transactions on electronic computers February 1965.

[8]Mudhafar A. Hassan Ali, Student Member, Zeee, Falah J. Hassan-Alshiroofi and Hemant G. Rotithor, senior member, "A Framework for Design of Multivalued Logic Functions and Its Application using CMOS Ternary Switches" IEEE transactions on circuits and systems-i: fundamental theory and applications, vol. 43, no. 4, April 1996.

[9]Moiez A. Tapia, "Solution of multivalued logic algebra equations" Electrical & Computer Engineering University of MIAMI Coral Gables, Florida Proceedings -1989 Southeastcon Ch2674-5/89/0000-0245$01.0001989 IEEE.

[10] Mrs. Rawnaq A. Habeeb "Coding-Decoding Ternary Logic" Electrical Engineering Department/College of Engineering/ Basrah University/Iraq Iraq J. Electrical and Electronic Engineering Vol.10 No.1, 2014.

[11]D.J.Porat "Three valued digital system" Proc.IEE Vol.116, No6, P.947-955, June 1969.

[12] X.W. Wu Prof. F.p. Prosser "CMOS Ternary Logic Circuits". PhD IEE proceedings, vol. 137, pt. G, no. I, February 1990.