Two Digit Parallel Analog To Ternary Converter

A.P.Dhande
Department Of Electronics & Telecommunication Engineering
Pune Institute Of Computer Technology, Pune, India
ashwindhande@pictsctr.edu

V.T.Ingole
Department Of Electronics & Telecommunication Engineering
College Of Engineering Badnera, India
vijayingole@hotmail.com

Abstract

The purpose of this paper is to present design architecture of two digit analog to ternary converter (T-ADC) and its simulation results. Proposed T-ADC operates at +/- 5v and is designed using analog comparators & ternary C-MOS logic gates. This T-ADC has conversion time of 100ms & does not require any d.c. level shifting of analog signal, as it requires in conventional ADCs. As an extension to this work, design of three digits T-ADC with encoder logic equations is also proposed.

1.Introduction

Ternary or base-3 logic system has several important advantages over binary logic in digital system. It can be summarized as reduction in the number of interconnections required to implement the logic functions; there by reducing chip area, more information contents can be transmitted over a given set of lines, lesser memory requirement for given data length. Besides this serial & some serial-parallel operations can be carried out at higher speed [1][2][3]. Its advantages have been confirmed in the various applications like memories, communications, arithmetic circuits & signal processing [4].

Emerging standards for digital communication or signal processing requires analog to digital converters. In this contribution, the T-ADC suitable for C-MOS digital processes is developed. It has $3^2 = 9$ quantization levels with 2-digit ternary output. An illustrative example is also considered for 4 KHz modulating signal at 8 KHz Sampling rate.

An organization of the paper is as follows. T-ADC block diagram & implementation is given in section II. Section III describes working and device parameters of T-ADC, Simulation results are given in section IV.Finally conclusion and 3-digit ADC design is considered.

II. Block Diagram & Implementation

The block diagram for parallel T-A/D converter is shown in fig.1 with its implementation in fig.2.Table 1 describes truth table for implementation in fig.2. The ternary logic states are represented by voltage levels as:

-5v = 0
0v = 1
+5v = 2

Since it is 2digit ADC it requires 3^2-1= 8 comparators. The analog samples are simultaneously applied to non-inverting terminals of all comparators. The other input to the comparators are d.c. reference voltages, which are available at each node of resistive divider network .The comparators 8,7,6&5 have positive reference voltages whereas 4,3,2 &1 have negative reference voltages. This arrangement avoides the need for adding d.c. shift to analog signal level. The magnitude of comparison voltage at any particular node is a function of node location on resistive divider network. Fig.3 shows analog voltage comparison with reference voltages & fig 4. is sample/hold circuit for proposed ADC.

Encoder is implemented using AND & OR ternary gates as proposed in reference [3]. Input to the encoder is output of comparators, which is either 2 (+Vsat) or 0 (-Vsat). Table 1 describes ternary digital output with respect to analog input to the comparators. The output logic equations of encoder are

$Y1 = X_6.X_5 + 1^* (X_1.X_2.X_3)$

$Y0 = X_8.X_7 + \overline{X}_6.X_5 + \overline{X}_3.X_2 + 1^*(X_1.\overline{X}_2 + X_4.\overline{X}_5 + X_7.\overline{X}_8)$

The terms X_1, $X_2 \ldots X_8$ are the output of comparators 1,2…8 respectively.

Sample and hold circuit employs C-MOS enhancement transistors and buffers. For 8KHz clock capacitor value = 0.1pf, sampling time = 12.5ms & hold time = 100ms.Here flat top sampling technique is adopted to sample the analog signal.

III.Working principle & Device parameters

With the proper reference voltages at each of the inverting terminals of comparators, output of comparators switches according to table 1. Each of the node voltage is compared with analog input V_A by comparators. Table2 describes switching conditions of comparators. Here V_R is the reference voltage at the node of resistive divider network.

Analog Voltage	Output
$V_A > V_R$	+Vsat
$V_A < V_R$	-Vsat
$V_A = V_R$	previous state

Table 2 Comparator Output

For a given analog sample level, all comparators below certain point in resistive network have one particular state and those below that point have opposite state. This pattern of 2 (+Vsat) & 0 (-Vsat) is applied to encoder circuit, which produces required digital ternary words in accordance with the bit pattern as shown in table 1 with output voltages. Table 3 describes comparator parameters used for simulation.

Comparator Parameters	
Slew Rate	20 v/μs
Output Voltage Swing	+/- 5v
Power Supply	+/- 5v

Table 3 Comparator Parameter

C-MOS ternary logic gates are implemented using P & N channel enhancement mosfet with threshold voltage V_T as 0.3v and drain ohmic resistance as 100KΩ for inverter.

IV. Simulation Results

All simulation results reported in this paper is obtained using electronic workbench Ewb50 version 5 with clock frequency 8KHz and supply voltages equal to +/- 5v. Table 4 summarized the parameters of proposed ADC.

Step Size	1.1v
Output Levels	9
Resolution	2 Digit
Conversion Time	100ms

Table.4 ADC Parameters

The graph in fig 5 & 6 displays corresponding ternary outputs with respect to analog input of 5v peak, at 8KHz sampling rate. In fig.7 comparative analysis is made with reference to circuit implementation using binary gates. Finally fig.8 is quantized ternary output

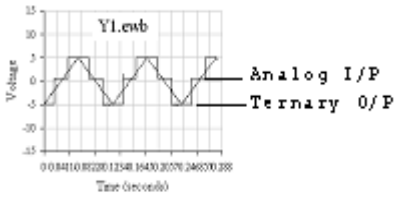

Fig.5 Simulated Output for Y1

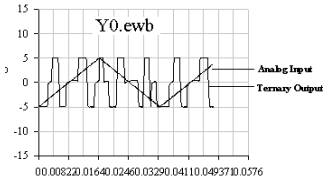

Fig6 Simulated Result for Yo

Fig.6 Simulated output for Y0

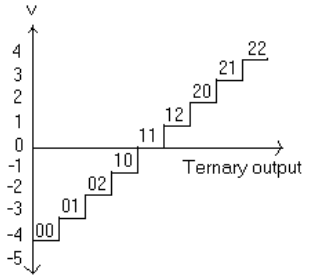

Fig. 7 Ternary output levels

Circuit	Proposed T-ADC	Based on binary gates [5]
No.of Gates	19	20 & Two switching transistor
Power dissipation	26mw Max. for full digit output	——
Conversion time	100 ms	120ms
output level	-v 0 +v	0 v/2 v

Fig.8 Comparison of proposed circuit with corresponding Circuit using binary gates

V. Conclusion

Since ternary logic offers several advantages over binary logic system, purpose of designing T-ADC is to generate ternary digital words which can be processed by ternary ALU to achieve reduction in circuit complexity, high bit rate etc.

The T-ADC proposed in reference [5] is based on binary to ternary encoding techniques, which requires binary logic gates, and binary to ternary encoder. Besides this T-ADC in [5] needs d.c. level shifting of analog signal, which gives positive value for all ternary states and increases conversion time.

The proposed T-ADC overcomes the above limitations, which reduces conversion time and relatively cost. Thus our T-ADC is appropriate for communication, signal processing & instrumentation.

VI. Future Advancement

With the proposed ADC, 9 quantized levels are possible. If quantized levels are to be increase, ADC with 3digit, 4digit with quantized levels 27,81 respectively can be achieved but it increases number of comparators and decoding circuit becomes little complex. With 27 quantized levels 26 comparators are required with encoder output equations as

$Y2 = X_{17}.X_{16}+1.\ (X_1.X_8)$

$Y1=\overline{X_{22}}X_{23}+X_{14}X_{13}+X_5X_4+1*(\overline{X_{22}}X_{10}+X_{11}\overline{X_{14}}+\overline{X_5}X_1+X_2\overline{X_1})$

$Y0=X_1\overline{X_4}+X_7\overline{X_{10}}+X_{10}\overline{X_{13}}+X_{16}\overline{X_{19}}+\overline{X_{22}}\overline{X_{25}}+1*$

$(\overline{X_2}X_3+X_6\overline{X_9}+\ X_{12}\overline{X_{15}}+X_{18}\overline{X_{21}}X_{23})$

The experimental results are carried out at +/- 5v enhancement MOSFET, however further advancement is possible with 3.3v MOSFET technology.[7]

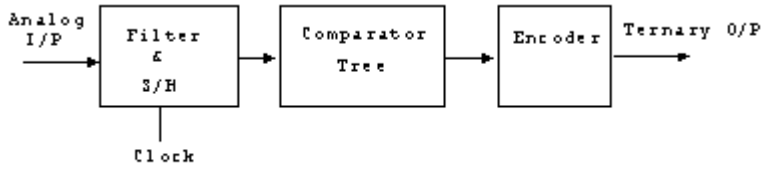

Fig.1 Architecture of T-ADC

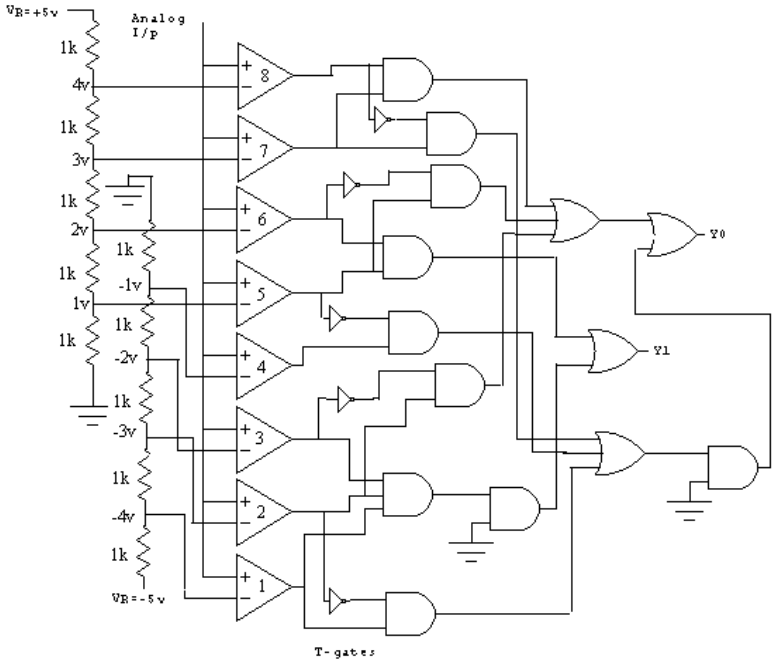

Fig.2 Implementation of T-ADC

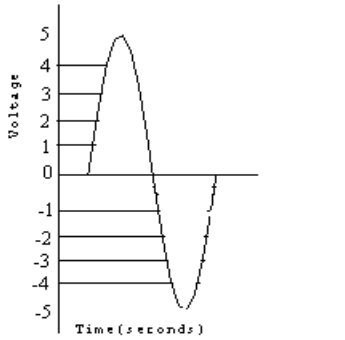

Fig.3 Analog voltage comparison

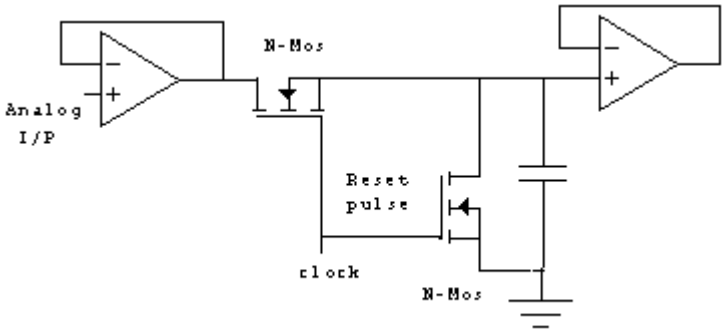

Fig.4 S/H Circuit

Analog I/P	Comparator O/P								Ternary O/P	
	8	7	6	5	4	3	2	1	Y1	Y0
4-5v	2	2	2	2	2	2	2	2	2	2
3-4v	0	2	2	2	2	2	2	2	2	1
2-3v	0	0	2	2	2	2	2	2	2	0
0-2v	0	0	0	2	2	2	2	2	1	2
0-0v	0	0	0	0	2	2	2	2	1	1
0--2v	0	0	0	0	0	2	2	2	1	0
-2--3v	0	0	0	0	0	0	2	2	0	2
-3--4v	0	0	0	0	0	0	0	2	0	1
-4--5v	0	0	0	0	0	0	0	0	0	0

Table-1 Truth Table for T-ADC

VII. References

1) D.I.Porat "Three valued digital system" Proc.IEE Vol.116, No 6, PP.947-966, June 1969.
2) K.C.Smith "The Prospects Of Multi-Valued Logic Technology & Application View" IEEE Transaction

   On Computer, Vol. -c-30, PP-619-627, Sept.1981.
3) P.C.Balla & A.Antoniou"Low Power Dissipation MOS Ternary Logic Family" IEEE Journal On Solid State Circuits Vol. SC-19 No.5 PP.739-749, October 1984.
4) S.L.Hurst "Multivalued Logic -Its Status & Future" IEEE Transaction on Computer, Vol C-33 PP.1160-1179, 1984.
5) N.E.Berbat & M.A.H. Abdul-Karim " A simultaneous Analog To Ternary Converter" Proceedings ISMVL 1979 PP.73-75
6) John D. Lenk "Simple Design Of Data Converters" EDN Series For Design Engineers.
7) K.W. Current & Y.B.Guo "Voltage comparator circuit for multiple valued CMOS logic" ISMVL 2002.