SMGroup

CHAPTER 3

Ternary Logic Families

INTRODUCTION

Ternary logic is implemented in two operating modes; these are current & voltage mode operation. In current- mode circuits, currents are defined to have logical levels that are integer multiples of a reference current (or logic 0 current) unit. The frequently used linear sum operation can be performed simply by wiring, resulting in a reduced number of active devices in the circuit. Where as in voltage mode circuits, distinct voltage levels are defined and device switches at their distinct levels. Voltage mode operation is again classified in to balance and unbalance operation mode. In balance mode, –v as (logic 0), reference ground (logic 1) and + v (logic 2) levels are there and in unbalance mode, reference ground (logic 0), v/2 9logic 1) and v (logic 2) levels are expressed. In this chapter unbalance voltage mode operation is considered for the operation of ternary families.

The basic switching elements used for the implementations of MVL in both the modes are Diode, transistors, MOSFETS & Resonant tunneling devices (RTDs) and recently Carbon Nano Tube (CNT) [1] and circuits are developed and simulated using MOS, RTD and CNT devices.

TERNARY LOGIC CIRCUITS BASED ON CMOS

Switching elements in the implementation of inverters those discussed in chapter1 are transistors, MOSFET & RTDs. Because of low power consumption, less propagation time, high fan in\out, high voltage swing & operation in GHz domain, circuits based on MOSFET of RTDs are more in use [2,3].

Figure 3.1 shows MOS base three inverters namely STI (simple ternary inverter), PTI (positive ternary inverter) &NTI (negative ternary inverter). Truth table for the same is given in Table 3.1

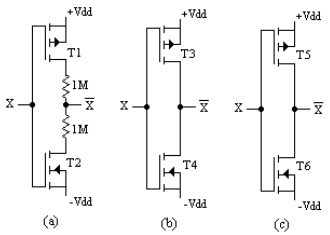

Figure 3.1: CMOS T-Inverter (a) STI (b) PTI (c) (NTI)

Table 3.1: Truth table for Inverter

Input X	Output		
	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

Operation of CMOS T- Inverter

Figure 3.1 (a) shows circuit realization of STI. The behavior of circuit is strongly dependent on choice of supply voltage, the logic levels V_H,V_I,V_L technological process parameter V_T and body effect on transistor. In this circuit T_1 is P Channel enhancement & T_2 is N channel enhancement transistor with drain ohmic resistance of $1x10^6$ Ω. The supply voltages are ± V_{dd} and three ternary levels as shown in table 3.2 for the operation of circuit, threshold voltage V+ has to satisfy the inequality

$$| -V_{dd} | < | V_T | < | +V_{dd}| \quad (1)$$

Assuming ± Vdd = ± 5V V_T should be ≅ 0 v

If condition 3.1 is satisfied & input X = high (V_H) is applied to input terminal, then T_2 turns ON (Vgs > V_T) and T1is OFF. Therefore output Vo ≅ -V_{dd} i.e. low (V_L). Since T_1 and T_2 are in series, current I_{D1} is drain current of T_1which is negligible.

When intermediate level V_I is applied to input X, Then $T_1$and T_2 are ON and output is ≅ V_LIf applied input is low, then T_1 turns ON and T_2 is OFF, so the output is ≅ +$V_{dd.}$

Table 3.2: voltage level –V to +V.

Voltage level	Logic value
+V	2
0	1
-V	0

PTI & NTI circuits are shown in Figure 3.1 (b) and (c) respectively. In these circuits T_3,T_5 are P- channel enhancement MOS. T_4,T_6 are N- channel enhancement MOS. The threshold voltages V_T of T_3 and T_6 are required to satisfy inequality

$$0 \le | V_T | \le | +V_{dd} | \quad (2)$$

and for T_4, T_5

$$|+V_{cc}| \le | V_T | \le | 2V_{cc}| \quad (3)$$

The operation of circuits is same as that of STI.

Operation of CMOS T- OR / NOR

T- OR is a circuit that have X_1---X_n as input &Yo as output such that

$$T-OR = X1+X2----+Xn = Max[X1, X2---Xn] \quad (4)$$

and T- NOR has an output that is compliment as OR function i.e.

$$T-NOR=\overline{X1+X2-----Xn}=\overline{Max[X1,X2---Xn]} \quad (5)$$

T Inverter is a basic circuit that is used for implementing T-OR/NOR functions, depending upon the type of inverter used, the logic functions T-OR/NOR can be Simple ternary OR/NOR (ST-OR/NOR), Positive ternary OR/NOR (PT-OR/NOR) and Negative ternary OR/NOR (NT-OR.NOR). Figure 3.2 shows ST-OR & NOR circuits and Table 3.3 for the same is summarized.

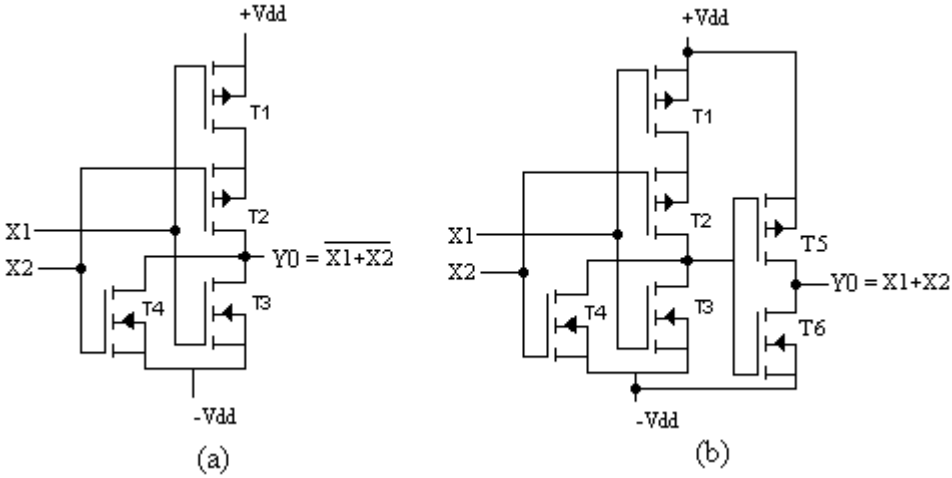

Figure 3.2: CMOS ST –NOR & ST – OR (a) ST-NOR (b) ST-OR.

Table 3.3: Truth table for Ternary OR/NOR Logic functions.

X_1 X_2	ST-OR	PT-OR	NT-OR	ST-NOR	PT- NOR	NT-NOR
0 0	0	0	0	2	2	2
0 1	1	0	2	1	2	0
0 2	2	2	2	0	0	0
1 0	1	0	2	1	2	0
1 1	1	0	2	1	2	0
1 2	2	2	2	0	0	0
2 0	2	2	2	0	0	0
2 1	2	2	2	0	0	0
2 2	2	2	2	0	0	0

The inequality condition required for implementing PT-NOR is, For T_1, T_2

$$|0| < V_T < |V_{dd}| \quad (6)$$

For T_3,T_4

$$|V_{dd}| < |V_T| < |2V_{dd}| \quad (7)$$

and for NT-NOR T_1, T2

$$|V_{dd}| < |V_T| < |2V_{dd}| \quad (8)$$

T_3, T_4

$$|0| < |V_T| < |V_{dd}| \quad (9)$$

CMOS T- AND/NAND

Ternary AND function is defined as

$$T-AND = X1.X2 - - - - - Xn = Min[x1x2xn] \quad (10)$$

$$T-NAND = \overline{X1.X2 - - - - - Xn} = Min\overline{[x1x2xn]} \quad (11)$$

Truth table for Simple, Positive and Negative ternary is AND/NAND given in Table 3.4 and implementation is shown in Figure 3.3.

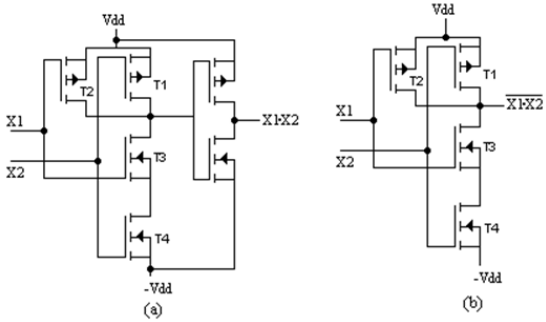

Figure 3.3: Implementation of Ternary AND/NAND (a) ST-AND (b) ST-NAND.

In the circuit implementation T_1,T_2,T_5 are P-Channel enhancement MOSFET &T_3, T_4, T6 are N-Channel enhancement MOSFET. The circuit is realized using inverters, in which T_1.T_2 are connected in Parallel & T_3, T4 are in series.

PT-AND/NAND& NT-AND/NAND are constructed by using PTI and NTI. However for implementation PT-NAND and NT-NAND inequality (6) (7) (8) and (9) should be satisfied.

Table 3.4: Truth table for ternary AND/NAND.

X_1 X2	ST-AND	PT-AND	NT-AND	ST-NAND	PT-NAND	NT-NAND
0 0	0	0	0	2	2	2
0 1	0	0	0	2	2	2
0 2	0	0	0	2	2	2
1 0	0	0	0	2	2	2
1 1	1	0	2	1	2	0
1 2	1	0	2	1	2	0
2 0	0	0	0	2	2	2
2 1	1	0	2	1	2	0
2 2	2	2	2	0	0	0

CMOS T-EX-OR/NOR

Ternary EX-OR/NOR function is defined as

$$T-EX-OR = X1 \oplus X2 \quad (12)$$

$$T-EX-NOR = \overline{X1 \oplus X2} \quad (13)$$

Basically functions in eq. (3.12) and (3.13) are mod 3 addition of ternary numbers neglecting the carry. Table 3.5 is a table for T-EX-OR /NOR operation. Operations can be verified using truth table.

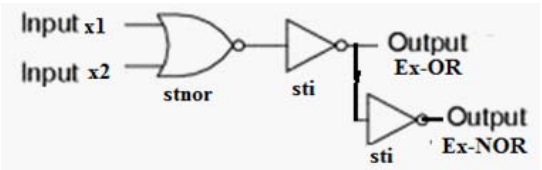

Figure 3.4: Gate level implementation of Ex-OR/Ex-NOR.

Table 3.5: Truth table for ternary EX-OR/Ex-NOR gates.

Input $X_1 X_2$	Output EX-OR	Output EX-NOR
0 0	0	2
0 1	1	1
0 2	2	0
1 0	1	1
1 1	2	0
1 2	0	2
2 0	2	0
2 1	0	2
2 2	1	1

Noise Margins in T-Gates

For binary logic gates two noise margins are defined, one for logic level 0, and one for logic level 1. In ternary logic system on the other hand, four noise margins are necessary, one for logic level 0, two for logic level 1, and one for logic 2. These quantities are denoted by NM0, NM1, and NM2 are defined as

$$NM_0 = V_1^0 - V_0^0 \quad (14)$$

$$NM_1^- = V_{01}^- - Vi1^- \quad (15)$$

$$NM1^+ = Vi^{1+} - V_0^{1+} \quad (16)$$

$$NM_2 = V_0^2 - V_1^2 \quad (17)$$

Vi^{1+}= Maximum gate input which will unambiguously be interpreted by the gate as level 0(1).

$Vi1^-$ = Minimum gate input which will unambiguously be interpreted by the gate *as* level 2(1).

V_0^{1+} = Maximum voltage which will appear at the gate output when the output is at logic level 0(1).

V_{01}^- = Minimum voltage which will appear at the gate output when the output is supposed to be logic level 2(1).

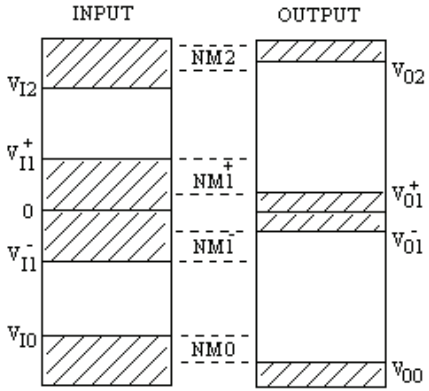

Figure 3.5: Noise margin in ternary logic gates.

The input voltages of Figure 3.5 can be expressed in terms of the threshold voltages as

$$V_{10} \approx | Vdd| - | V_{TE} | \quad (18)$$

$$Vl_1 \approx - | V_{TD} | \quad (19)$$

$$Vl_1 \approx | V_{TD} | \quad (20)$$

$$Vl_2 \approx | V_{TE} | - |V_{CC} | \quad (21)$$

Therefore, ([3.14)to (3.17) yield

$$NM_0 = 2Vdd - | V_{TE} | \quad (22)$$

$$NM_1 = | V_{TD} | \quad (23)$$

$$NM_1 = | V_{TD} | \quad (24)$$

$$NM_2 = 2Vdd - | V_{TE} | \quad (25)$$

VOLTAGE AND CURRENT PARAMETERS

For the T gates explained above, the voltage and current parameters are proposed below based on our simulation results.

- High level input voltage (V_{IH}). Minimum input voltage, which is recognized by the gate as logic 2. = 4.35v

- Intermediate level input voltage (V_{II}^{+}): Minimum input voltage, which is recognized by the gate as logic 1. =1v.
- Intermediate level input voltage (V_{II}^{-}): Minimum input voltage, which is recognized by the gate as logic 1. = -1v.
- Low level input voltage (V_{IL}): Maximum input voltage, which is recognized by the gate as logic 0. = -3.5 v.
- High level output voltage (V_{OH}): This is the minimum voltage available at the output corresponding to logic 2. = 5.0V.
- Intermediate level output voltage (V_{OI}^{+}): This is the minimum voltage available at the output corresponding to logic 1. = 14.78mV.
- Intermediate level output voltage (V_{OI}^{-}): This is the minimum voltage available at the output corresponding to logic 1. = -14.9mV.
- Low level output voltage (V_{OL}): This is the maximum voltage available at the output corresponding to logic 0. = -5.0 v.
- High level input current (I_{IH}): This is minimum current, which must be supplied by driving source corresponding to logic 2. = 1μA.
- Intermediate level input current (I_{II}): This is minimum current, which must be supplied by driving source corresponding to logic 1. = 4.44 μA.
- Low level input current (I_{IL}): This is maximum current, which must be supplied by driving source corresponding to logic 0. = -1μA.
- High level output current (Io_{H}): This is maximum current which gate can source corresponding to logic 2. = 4.9 μA.
- Intermediate level output current (Io_{I}): This is maximum current which gate can sink corresponding to logic 1. –0.049μA.
- Low level input current (Io_{L}): This is maximum current which gate can sink corresponding to logic 0. = -4.9 μA.

CALCULATED NOISE MARGIN

From above voltage & current parameters noise margin for logic gates are

- Noise margin corresponding to logic 0: $NM_0 = V_{OL} - V_{IL} = 0.65$ V
- Noise margin corresponding to logic 1: $NM_1^{+} = V_{II}^{+} - 0 = 14$mV
- Noise margin corresponding to logic 1: $NM_1^{-} = V_{II}^{-} - 0 = 14$mV
- Noise margin corresponding to logic 2 : $NM_2 = V_{OH} - V_{IH} = 0.65$V

Device Switching Time

It is defined as speed at which MOSFET changes its state from off-intermediate-on state & vice versa. It is expressed in terms of propagation delayτ. Switching time for above devices is shown for N-channel and P=channel MOSFET in Figure 3.6.

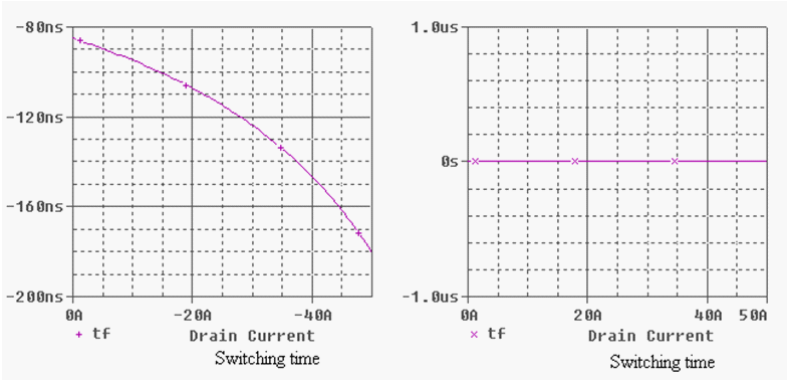

Figure 3.6: Switching time for N and P channel MOSFET.

Power Dissipation

It is amount of power dissipated in single gate. It is a arithmetic addition of static power, dynamic power and power during transition of MOS from ON to OFF state and vice versa. For inverter, maximum power will dissipated only when both transistors T1 & T2 are ON. Dynamic power dissipation during transition is almost negligible. So power dissipation is

$$P.D = \frac{Vdd^2(R1+R2)}{(R1.R2)}$$

For supply = +/- 5v & R_d = 1M each, P.D. 100 μW. Here R1 and R2 form parallel combination of equivalent R_d.

Same analogy is extended for P.D. calculation in NAND/NOR T- gates. A Simulated values are about 10 to 12 W and for AND/OR is 10 to 12μW.

TERNARY LOGIC CIRCUITS BASED ON RTDS

Resonant-Tunneling Diodes (RTDs) show Negative Differential Resistance (NDR) at room temp. If InGaAs /AlAs double barrier structure are used, Peak current densities as high as 10^5 A/m2 are obtained with peak to valley current ratio more than five The NDR Characteristic can be used to reduce circuit complexity; enhance circuit Performance in terms of speed, chip area & Power consumptions.

One of the possible implementations of MVL circuit is using RTDs & high electron mobility transistors (HEMT). The basic idea of these circuits is to synthesize transfer characteristic by

two-logic element namely up & down literal, that is obtained by using circuits called monostable-to-bistable transition element (MOBILE) [4].

MOBILE exhibits two functions i.e. down & up literal. Up &DOWN literals are one variable function with binary output. The down literal is high for x < a & for x > a, while up literal is low for x < a & high for x > a, where x & a are threshold value & variable respectively. By using these circuits as key element MVL circuits are implemented.

Circuits Elements: Down & Up Literals

A MOBILE basically consists of two series-connected RTDs, A and X, as shown in Figure 3.7 (a) It is assumed that X has a gate to modulate its peak current. Oscillating voltage between V_1 (low) and V_2 (high) is supplied to the circuit. The output is obtained at every cycle of oscillation Figure 3.7 (b). When the circuit voltage V_{CLOCK} is V_1, the circuit is monostable, where both RTD's are in the "on" (low- resistance) state. As V_{CLOCK} increases from V_1 to V_2, the circuit evolves from the monostable state to the bistable state Figure 3.7(c).

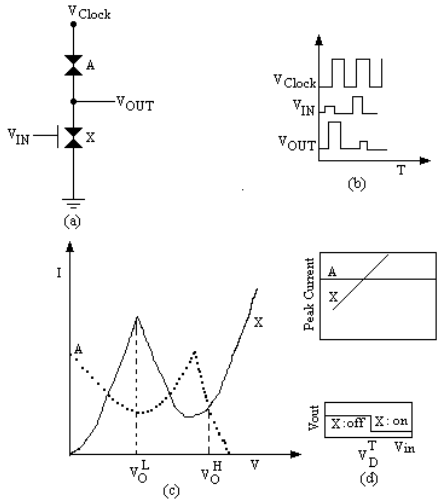

Figure 3.7: (a) Circuit configuration for down-literal monostable-to-bistable transaction logic element (MOBILE).

(b) A timing chart of the operation. (c) The bi-Stable state and (d) peak currents as a function of input voltage and transfer Characteristics of down literal.

V_2 is selected as a value so that either A or X switches from the "on" state to the "off" state (high–resistance) state when $V_{CLOCK} = V_2$. If X switches into the "off" state and A remains in the "on" state, the output is V_0^H (high) because the voltage between the terminals of X increases as X switches off. On the other hand, it A switches off and X remains on, the output is V_0^L (low). The output is thus determined at the rising edge of V_{CLOCK} and latched until V_{CLOCK} decreases from V_2 to V_1, when the circuit is reset and ready for the next cycle.

Suppose that the peak current of X increases with an increase in the gate voltage V_{IN} as shown in Figure 3.7 (d). To obtain the logic function, the input V_{IN} is first supplied to the gate and then V_{CLOCK} increases from V_1 to V_2. If $V_{IN} < V_T^D$, X switches from "on" to "off" according to switching rule: the smaller the peak current the earlier the RTD switches as the circuit voltage increases. Therefore, the output is V_0^H (high) as explained above. On the contrary, if $V_{IN} > V_D^T$, the peak current of A is smaller than that of X. Then A switches to the "off" state, and the output is V_0^L (low). In this manner, the circuit works as an inverter with a threshold of V_T^D Figure 3.7 (d) shows that the threshold voltage is determined by the intersection of two lines representing the peak currents. If we increase the RTD area of A, for example the line denoted A in Figure 3.7 (d) moves upward and V_T^D increases. The threshold is thus tunable. If the threshold is adjusted to a properly selected value by designing the device geometry, the circuit operates as a down literal.

In a similar manner an up literal is obtained with the circuit shown in Figure 3.7. Here, the peak current of Y can be modulated by the gate voltage $V_{IN.}$ As shown in Figure 3.8 (a), it is assumed that the peak current of Y increases as V_{IN} increases and becomes larger than that of B when $V_{IN} > V_T^U$. As the circuit voltage increases from V_1 to V_2, Y switches off when $V_{IN} < V_T^U$, according to the switching rule mentioned above B remains "on," and the output is V_0^L (low). If $V_{IN} > V_T^U$, B switches from the "on" state to the "off" state and the output is V_0^H (high). Therefore, the circuit operates as an Up literal.

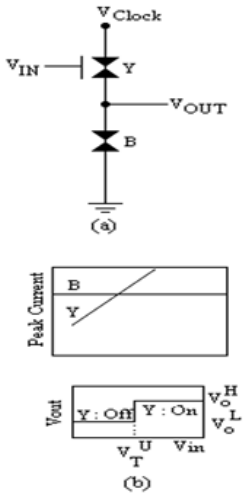

Figure 3.8: (a) Circuit configuration of Up literal (b) Peak current as a function of input voltage & Transfer characteristics of Up literal.

Operation of RTD T-Invertor

By combining up & down literal, transfer characteristic that represent multilevel output can be synthesized. Ternary inverters, that forms the complementation in 3-valued logic is implemented by using two down literals.

Figure 3.9 shows the circuit configuration on which contains two down literals. A pair of A and X and a pair of B and Y. The output terminal is extracted from the node between B and X & the input terminal is connected to the gates of X and Y. The upper limit of V_{CLOCK}, V_2, has been selected to that two out of the four RTD's, A, B, X, and Y, switch off at V_2. If the two RTD's that switch off are X and Y, the voltages between the terminals of X and Y increase and the output is the highest. If either X or Y switches off at the output is the second highest, because the voltage only increases between the terminals of either X or Y. If both X and Y remains unswitched, the output is the lowest. The output voltage thus quantized into three discrete levels is obtained then $V_{CLOCK} = V_2$.

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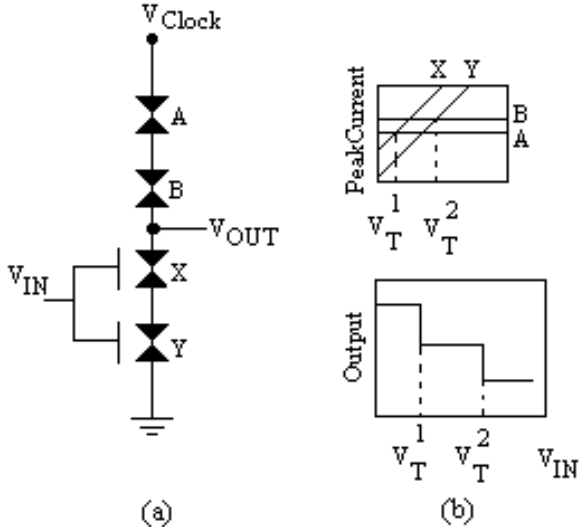


Figure 3.9: (a) Circuit configuration of ternary inverter and (b) peak currents as function of input voltage and transfer characteristics of a ternary inverter.

Logic operation is obtained as follows: Suppose that the peak currents of X and Y increases as the input increases and that the peak current of A is smaller than that of B, as shown in Figure 3.9 (b). As mentioned above, the circuit shown in Figure 3.9(a) consists of two down literals: one is the pair of A and X with threshold of V_T^1, while the other is B and Y with the threshold of V_T^2. The output is a superposition of these two down literals, as is explained below. If $V_{IN} < V_T^1$, the peak currents of X and Y are both smaller than those of A and B. Therefore, according to the switching rule in series-connected RTD's X and Y switch off when $V_{CLOCK} = V_2$, and the output is the highest at "2." When $V_T^1 < V_{IN} < V_T^2$, the peak current of A is smaller than that of X, and then A and Y switch off when $V_{LOCK} = V_2$. This results in the intermediate output value if "1." If $V_T^2 < V_{IN}$, the switched-off RTD's are A and B [X and Y remain unswitched], and the output is the lowest at "0." The relation between the input, switched RTD's and the output summarized in Table 3.6

Table 3.6: Input versus output in ternary Inverter.

V_{IN}	Switched RTD's	V_{OUT}
$V_{IN} < V_T^1$	X, Y	"2"
$V_T^1 < V_{IN} < V_T^2$	A, Y	"1"
$V_T^2 < V_{IN}$	A, B	"0"

Operation of RTD T-AND/ NAND Logic gates

Ternary inverters are combined to synthesis T-AND/NAND logic gates. Truth table for the AND/NAND Operation given in Table 3.4 Figure 3.10 shows implementation of T-AND/NAND gates. Four down literals that form the T-AND/NAND gate are a pair of A-X, B-Y, A^I -X^I&B^I -Y^I. Let for A-X &A^I -X^I threshold voltage be V_T^1& V_T^2 for B-Y, pair B^I -Y^I. The operation of circuit is same as if two pairs of inverters connected in parallel (A-B&A^I - B^I) & two in series (X-Y &A^I -X^I). Table 3.7 summarizes details of switching RTD's.

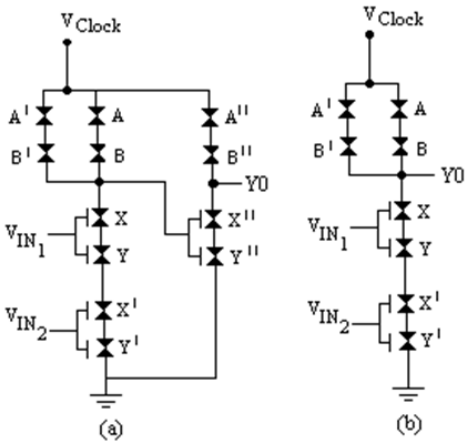


Figure 3.10: RTD based T-AND/NAND gates (a) AND (b) NAND.

Table 3.7: RTD switching table.

Vin_1	Vin_2	V_T^1	V_T^2	OFF	ON	OFF	ON	Yo	Yo
0	0	$Vin_1 < V_T^1$	$Vin_2 < V_T^2$	X-Y	A-B	X^I -Y^I	A^I-B^I	2	0
0	1	$Vin_1 < V_T^1$	$Vin_1 < Vin_2 < V_T^2$	X-Y	A-B	A^I -Y^I	B^I-X^I	2	0
0	2	$Vin_1 < V_T^1$	$Vin_2 > V_T^2$	X-Y	A-B	A^I-B^I	X^I-Y^I	2	0
1	0	$V_T^1 < Vin_1 <$ VT2	$Vin_2 < V_T^2$	A-Y	B-X	X^I-Y^I	A^I-B^I	2	0
1	1	$V_T^1 < Vin_1 <$VT2	$Vin_1 < Vin_2 < V_T^2$	A-Y	B-X	A^I-Y^I	B^I-X^I	1	1
1	2	$V_T^1 < Vin_1 < V_T^1$	$Vin_2 > V_T^2$	A-Y	B-X	A^I-B^I	X^I-Y^I	1	1
2	0	$Vin_1 > V_T^1$	$Vin_2 < V_T^2$	A-B	X-Y	X^I-Y^I	A^I-B1	2	0
2	1	$Vin_1 > V_T^1$	$Vin_1 < Vin_2 < V_T^2$	A-B	X-Y	A^I-Y^I	B^I-X^I	1	1
2	2	$Vin_1 > V_T^1$	$Vin_2 > V_T^2$	A-B	X-Y	A^I-B^I	X^I-Y^I	0	2

Operation of RTD T-OR/NOR logic gate

Function in the eq. (4) & (5) is implemented using, for down literals in series parallel connection as shown in Figure 3.11. This structure series as T-OR/NOR logic gate. Truth table for OR/NOR logic function is given in Table 3.5.

Let for A-X &A^{l} -X^{l} threshold voltage be V_T^1& V_T^2 for B-Y, B^{l}-Y^{l} pair. Table 3.8 gives switching table for RTD's. Assuming clock is applied such that any four of RTS's are off when V_2 is maximum. The switching of RTD's can be verified for different input conditions Vin_1, & Vin_2. Symbols for T-OR/NOR gates are shown in Figure 1.5 [5,6]

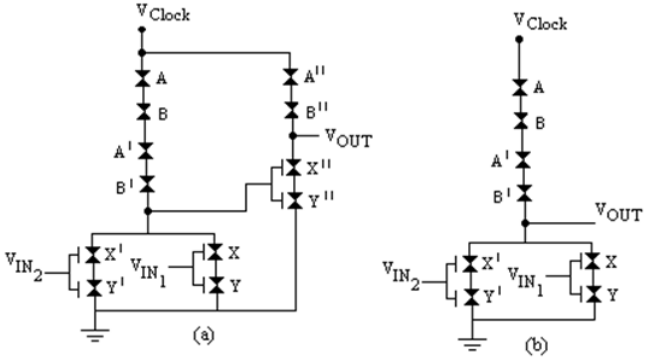


Figure 3.11: RTD based OR/NOR gates (a) OR (b) NOR.

Table 3.8: RTD switching table.

Vin_1	Vin_2	V_T^1	V_T^2	OFF	ON	OFF	ON	YO	YO
0	0	$Vin_1 < V_T^1$	$Vin_2 < V_T^2$	X-Y	A-B	X^{l} -Y^{l}	A^{l}- B^{l}	2	0
0	1	$Vin_1 < V_T^1$	$V_T^1 < Vin_2 < V_T^2$	X-Y	A-B	A^{l} -Y^{l}	B^{l}- X^{l}	1	1
0	2	$Vin_1 < V_T^2$	$Vin_2 > V_T^2$	X-Y	A-B	A^{l} -B^{l}	X^{l}Y^{l}	0	2
1	0	$V_T^1 < Vin1 < V_T^2$	$Vin_2 < V_T^2$	A-Y	B-X	X^{l} - Y^{l}	A^{l} - B^{l}	1	1
1	1	$V_T^1 < Vin1 < V_T^2$	$V_T^1 < Vin_2 < V_T^2$	A-Y	B-X	A^{l}- Y^{l}	B^{l}- X^{l}	1	1
1	2	$V_T^1 < Vin1 < V_T^2$	$Vin_2 > V_T^2$	A-Y	B-X	A^{l} - B^{l}	X^{l} - Y^{l}	0	2
2	0	$Vin_1 > V_T^1$	$Vin_2 < V_T^2$	A-B	X-Y	X^{l} - Y^{l}	A^{l} - B^{l}	0	2
2	1	$Vin_1 > V_T^1$	$V_T^1 < Vin2 < V_T^2$	A-B	X-Y	A^{l} - Y^{l}	B^{l}- X^{l}	0	2
2	2	$Vin_1 > V_T^1$	$Vin2 > V_T^2$	A-B	X-Y	A^{l} - B^{l}	X^{l} - Y^{l}	0	2

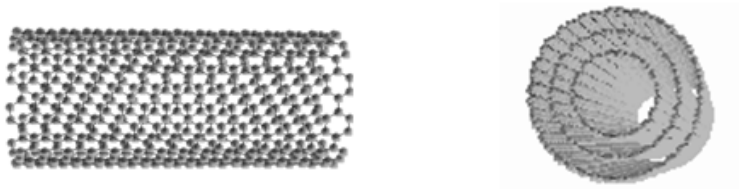
TERNAY LOGIC GATES BASED ON CARBON NANO TUBE TECHNOLOGY

Recent advancement in ternary logic gate is based on Carbon Nano Tube (CNT) technology. CNTs attribute a number of extraordinary properties, amongst which are high electric conductivity, high thermal conductivity, mechanical strength, thermal resistivity / stability, actuation properties at low voltages and field emission. An existing semiconductor technology

has limitations on its performance like, electron tunneling through short channels and thin insulator films, the associated leakage currents, passive power dissipation, short channel effects, and variations in device structure and doping. These limits can be overcome to some extent and facilitate further scaling down of device dimensions by modifying the channel material in the traditional bulk MOSFET structure with a single carbon nanotube or an array of carbon nanotubes [7].

Carbon nanotube (CNTs) is form of carbon with a cylindrical nanostructure. Nanotubes have been constructed with length-to-diameter ratio of up to 132,000,000:1, significantly larger than for any other material. These cylindrical carbon molecules have unusual properties, which are valuable for nanotechnology, electronics.

There are two forms of CNT i.e. single walled and multi walled. Wall is a layer of substance molecules. Depending upon the layers it is referred to as single walled and multi walled Nano tube. Figure 3.12 (a) and (b) shows single and multi walled Nano tubes.



(a) (b)

Figure 3.12: (a) Single walled, (b) Multi walled Nano tube.

Single-walled nanotubes (SWNT) have a diameter of close to 1 nanometer, with a tube length that can be many millions of times longer. The structure of a SWNT is conceptualized by wrapping a one-atom-thick layer of graphite called graphene into a seamless cylinder. The way the graphene sheet is wrapped is represented by a pair of indices (*n*,*m*). The integers *n* and *m* denote the number of unit vectors along two directions in the honeycomb crystal lattice of graphene. If *m* = 0, the nanotubes are called zigzag nanotubes, and if *n* = *m*, the nanotubes are called armchair nanotubes. Otherwise, they are called chiral. The diameter of an ideal nanotube can be calculated from its (n,m) indices as in Figure 3.13.

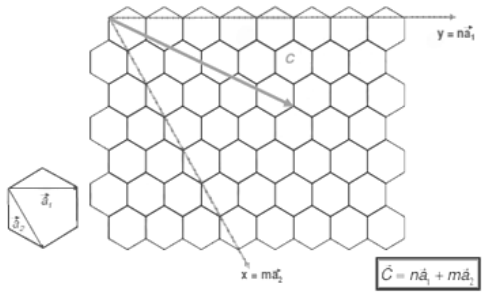


Figure 3.13: Structure of single walled CNT.

CNT based Field Effect Transistor

As one of the promising new devices, carbon nanotube FETs (CNTFETs) avoid most of the fundamental limitations for traditional silicon devices, due to their unique one-dimensional band-structure that suppresses backscattering and makes near-ballistic operation a realistic possibility [8-10]. A single walled CNT (SWCNT) can be visualized as a sheet of graphite, which is rolled up and joined together along a roll- up vector Figure 3.14(a).

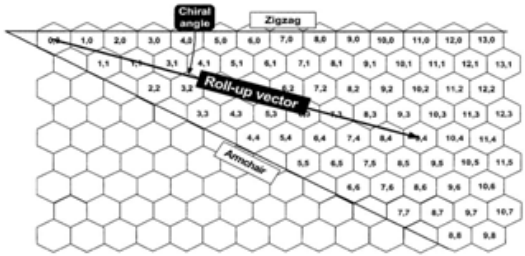
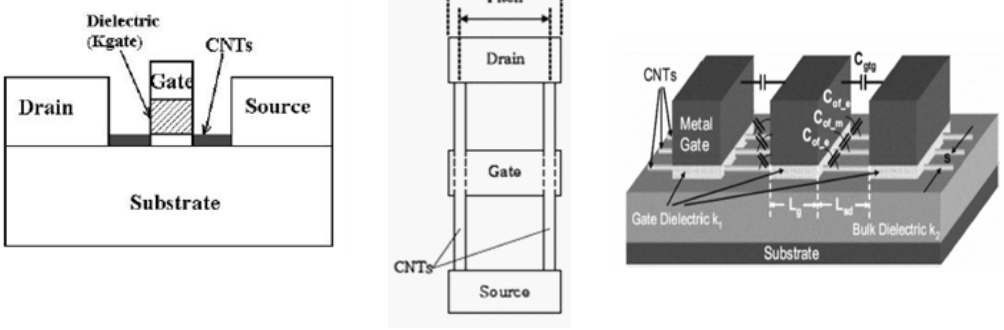


Figure 3.14(a)**:** Unrolled graphite sheet.

Depending on the chiral angle (roll-up vector or chirality vector), the CNT can be either semiconducting or metallic. By considering the indices (n, m) shown in Figure 1, the nanotube is metallic if n = m or n-m = 3i where i is an integer. Otherwise, the tube is semiconducting. CNTFETs are the FETs that make use of semiconducting CNTs as channel material between two metal electrodes that act as source and drain contacts. The operation principle of CNTFET is similar to that of traditional silicon devices. CNT structure is shown in Figure 3.14 (a),(b) and (c) respectively. As shown in Figure 3.14: (b), this three (or four) terminal device consists of a semiconducting nanotube, acting as conducting channel, bridging the source and drain contacts. The device is turned on or off electrostatically via the gate. Despite several serious technological barriers, CNTFETs with their small feature size and high-current capability show a potential for performance improvement compared with CMOS transistors.



a)2-D view b) cross sectional view c)3-D view

Figure 3.14(b)**:** CNT structure.

The CV/I performance of an intrinsic CNTFET is 13 times better than the CV/I performance of a bulk n-type MOSFET because the CNTFETs effective gate capacitance of one CNT per gate is about 4% compared to bulk CMOS and the driving current ability of each CNT is about 50% of a bulk n-type MOSFET with minimum gate width (48 nm) at a 32 nm node (due to the ballistic transport nature of a CNT). Moreover due to the similar behavior and the current driving capability of a pFET compared to those of an FET the performance improvement of a pFET over a PMOS is better than the one of a nFET over a NMOS. Even though a CNTFET has a leakage current in the off-state, this leakage current is controlled by the full band gap of the CNTs and the band to band tunneling; this is less than for a MOSFET [11,12].

The expected (optimistic) performance advantage of a CNTFET is unlikely to be achievable in a real device and will be significantly degraded for the CV/I (6 times for a nFET and 14 times for a pFET) due to device/circuit non-ideal conditions. These non-ideal conditions include the series resistance of the doped source/drain region, the Schottky Barrier (SB) resistance at the metal/CNT interface, the gate outer-fringe capacitance and the interconnect wiring capacitance. However, the need for low power consumption and high operating frequency has resulted in geometry and supply scaling with a significant increase in operating temperature for a device. With these scaling features, the effects of systematic and random variations in Process, supply Voltage, and Temperature (PVT) may cause an inconsistent delay and increase in leakage to appear even in low power circuits, thus becoming one of the major challenges in nanoscale devices. Figure 3.15 shows V-I (Ids Vs Vgs) characteristic for 18 nm CNTFET.

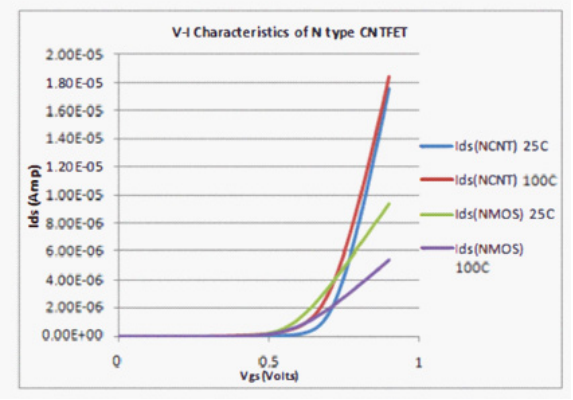


Figure 3.15: V-I characteristics of 18nm CNTFET.

CNT based Ternary Logic Gates

I: CNT inverter and its operation

The operation of CNT inverter is same as that of semiconductor FET based inverter except an optimum performance is achieved in operation of the circuits when employed with CNTFET. Symbol for CNTFET is shown in Figure 3.16 and inverter implementation in 3.17(a), (b) and(c) as STI, PTI and NTI.

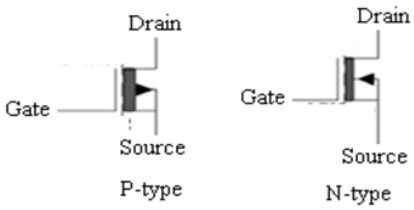


Figure 3.16: Symbols for P and N type CNTFET.

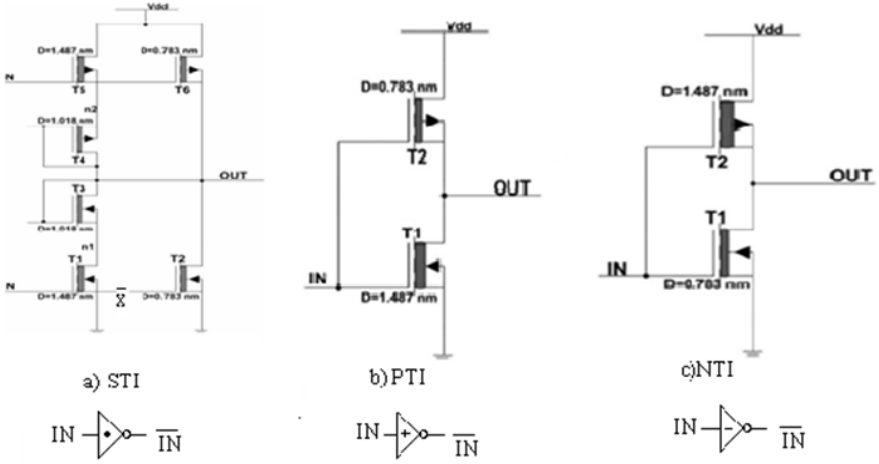
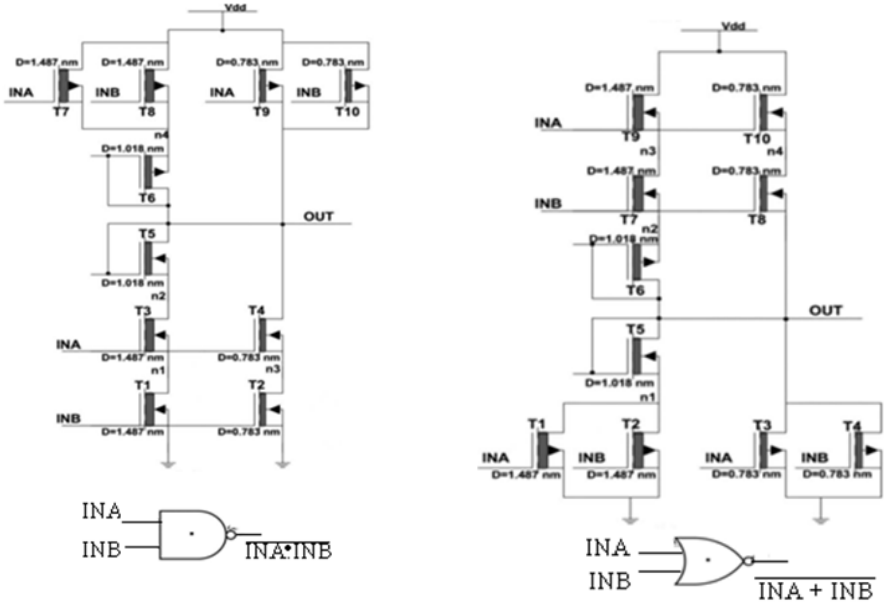


Figure 3.17: Implementation of CNT based inverter (a) STI (b) PTI (C) NTI.

Operation: One of the most widely used logic design style is static complementary CMOS; the main advantages of the complementary design are robustness, good performance, and low power consumption with small static power dissipation. A complementary CNTFET network can also be used for ternary logic design to achieve good performance, low power consumption, and to avoid the use of large resistors and reduce area overhead. Figure 3.15 shows the CNTFET-based STI design; the STI in Figure 3.17(a) consists of six CNTFETs. The chiralities of the CNTs used in T1, T2, and T3 are (19, 0), (10, 0), and (13, 0), respectively. From (1 given below), the diameters of T1, T2, and T3 are 1.487, 0.783, and 1.018 nm, respectively. Therefore, the threshold voltages of T1,T2, and T3 are 0.289, 0.559, and 0.428 V, respectively from (2 given below).The threshold voltages of T5, T6, and T4 are − 0.289,− 0.559,and − 0.428 V, respectively. When the input voltage changes from low to high at the power supply voltage of 0.9 V, initially, the input voltage is lower than 300 mV. This makes both T5 and T6 turn ON, bothT_1andT_2turn OFF , and the output voltage 0.9 V, i.e. logic 2. As the input voltage increases beyond 300 mV, T_6 is OFF and T5 is still ON .Meanwhile,T1is ON and T2 is OFF . The diode connected CNTFETs T4 and T3 produce a voltage drop of 0.45 V from node n2 to the output, and from the output to n1 due to the threshold voltages of T4 and T3. Therefore, the output voltage becomes 0.45 V, i.e., half of the power supply voltage.

As shown in Table I, half V_{dd} represents logic 1. Once the input voltage exceeds 0.6 V, both T5 and T6 are OFF, and T2 is ON to pull the output voltage down to zero. The input voltage transition from high to low transition is similar to the low to high transition [13].

II: CNT NAND and NOR gates



(a) (b)

Figure 3.18: carbon nanotube field-effect transistor-based NAND and NOR gates. (a) Circuit diagram for two-input NAND and its symbol. (b) Circuit diagram for two-input NOR and its symbol.

The circuits and symbols for the two-input ternary NAND and ternary NOR are shown in Figure 3.18(a) and (b), respectively. Each of these two gates consists of ten CNTFETs, with three different chiralities. They are essentially the same as their binary CMOS counterparts, except for the transistors of different threshold voltages. In these two gates, similar to the STI circuit of Figure 4, the transistors with diameters of 1.487, 0.783, and 1.018 nm have threshold voltages of 0.289, 0.559 and 0.428 V, respectively, as established using (2). Its operation is same as that of FET based TNANA and NOR gates [13].

Performance characteristic of CNT Logic Gate

Power delay product

Due to the increased demand for high-speed, high-throughput computation, and complex functionality in mobile environments, reduction of delay and power consumption is very challenging. Table 1 shows the delay, power, and PDP of logic gates in 32 nm CNTFET technologies; the PDP of the 32 nm MOSFET is about 100 times higher than that of the 32 nm CNTFET.

		Delay (sec)	Power (watt)	PDP (joule)
CNTFET	Inverter	2.42E-12	1.11E-07	2.69E-19
	NAND2	3.49E-12	1.89E-07	7.41E-19
	NAND3	5.06E-12	2.90E-07	1.47E-18
	NOR2	3.50E-12	1.85E-07	6.48E-19
	NOR3	5.08E-12	2.73E-07	1.39E-18

PDP: Power Delay Product; CNTFET: Carbon Nanotube Field-Effect Transistor

Leakage power

As process dimensions shrink further into the nanometer ranges, traditional methods for dynamic power reduction are becoming less effective due to the increased impact of static power [14]. In general, leakage power is different depending on the applied input vector. Figure 3.17 shows the maximum and minimum leakage power for 32 nm CNTFET based logic gates. Figure 3.17 also shows that the maximum leakage power shows a similar trend for both CNTFET based gates, while the minimum leakage power shows somewhat different trends, because the stack effect is reduced in CNTFET circuits.

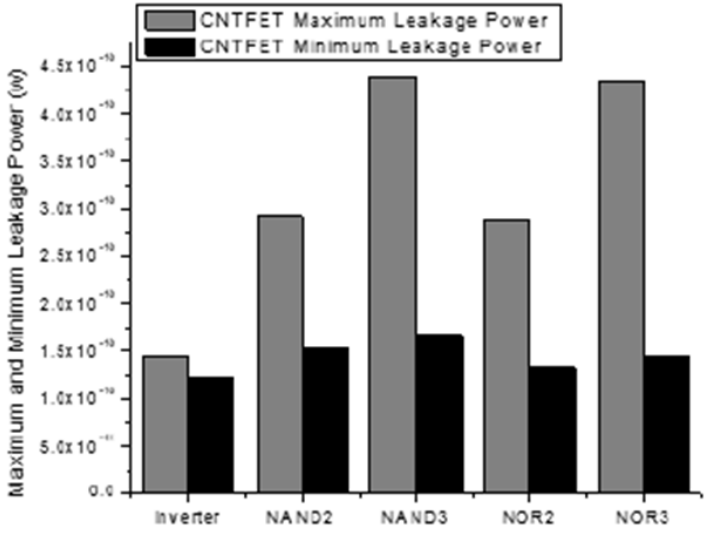


Figure 17: Maximum and minimum leakage power for 32 nm carbon nanotubeFET (CNTFET) logic gates.

Frequency response

For establishing the frequency response, AC simulation has been performed for CNTFET inverters. The results are given in Figure 3.18, where the CNTFET inverter shows nearly 3dB more voltage gain and 3 times higher 3dB frequency (f3dB).

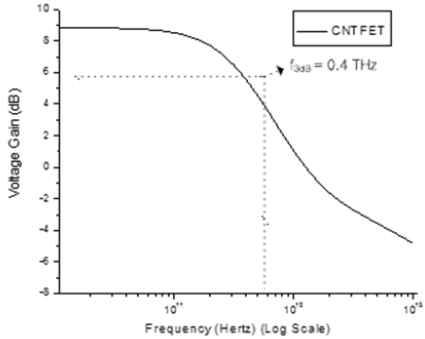


Figure 18: Frequency response for 32 nm metal-oxide semiconductor carbon nanotube FET (CNTFET) inverters.

PVT variations

With technology scaling, the effects of systematic and random variations in PVT have led to inconsistent delay and leakage in low power circuits, thus becoming a major obstacle for device scaling. Significant levels of process variations affect technology scaling beyond 90 nm, and they are changing the design environment from a deterministic to a probabilistic one. Moreover, the requirement of low power relies on supply voltage scaling, making voltage variations a significant challenge. The quest for increase in higher operating frequencies has resulted in significantly high junction temperature and within-die temperature variation [13,15,16]. Therefore, the possible performance degradation due to PVT variations has become a major criterion in assessing the performance of a new technology.

Process variation

When investigating physical process variations, CNTFET have different characteristics. The current change in CNTFET is below ±0.5%. However when the diameter of the CNTFET is changed by ±10%, the current change in a CNTFET is about ±17% as shown in Figure 3.19. Therefore for a CNTFET, the diameter variation is more important because a CNTFET is more sensitive to diameter variation than length and width variations. Based on this observation, the PDP and leakage of a CNTFET are computed and shown in Figure. 3.20 and 3.21, respectively. When the diameter of a CNTFET is changed, then the PDP changes too. Figure 3.21 shows that the maximum leakage power increases when the diameter is increased. Also note that the threshold voltage and diameter of a CNTFET are determined based on the chirality of the CNTs used in this type of transistor.

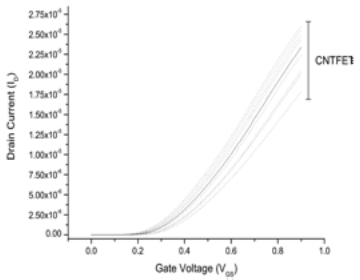


Figure 3.19: IDS (drain-to-source current) vs. VGS (gate-to-source voltage) with 10% Change of carbon nanotube (CNT) diameter (chirality) for the 32 nm CNTfield-effect transistor (FET).

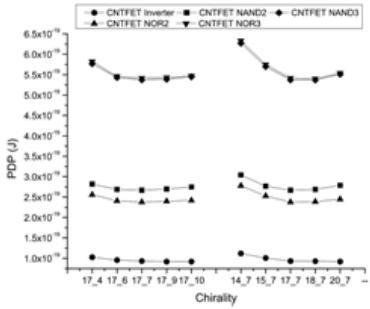


Figure 3.20: Power Delay Product (PDP) of 32 nm carbon nanotube field effect transistor (CNTFET) logic gates vs diameter (chirality) of CNT.

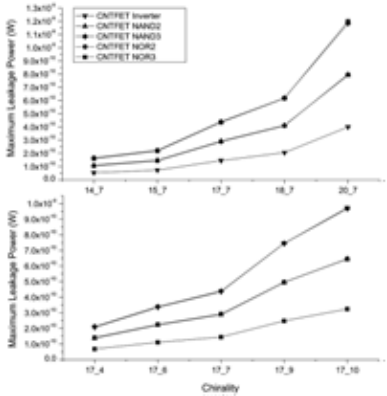


Figure 3.21: Maximum leakage power of the 32 nm carbon nanotube field effect transistor (CNTFET) logic gates vs. Diameter (chirality) of CNT.

Voltage variation

The reduction in power consumption due to voltage scaling is also confronted with the increased sensitivity to voltage variations; this is a major concern to assess the performance of a new technology such as CNTFETs. Figures 3.22 show the PDP for 32 nm CNTFET logic gates, respectively when the supply voltage is decreased until the gate stops functioning. These figures show that the inverter and the other logic gates operate until the supply voltage decreases to 0.5 V and 0.6 V, respectively. The overall PDP of the CNTFET-based gates is significantly low.

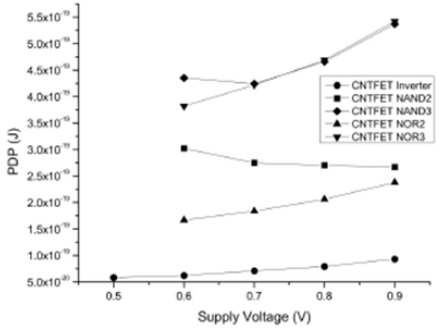


Figure 3.22: Power delay product (PDP) of 32 nm carbon nanotube field effect transistor

(CNTFET) logic gates vs. supply voltage.

Temperature variation

As the circuit speed increases, a larger power consumption is often encountered, thus resulting in more heat at chip level. Circuits with an excessive power dissipation are more susceptible to run-time failures and account for serious re- liability problems [13,16]. Figure 3.23 the PDP of the CNTFET logic gates is constant. Maximum leakage power for CNTFET-based gates increase is exponential. Few combinational circuits (such as a 4 stage inverter chain, a 2:4 decoder, a 4:16 decoder, the ISCAS-85 Benchmark Circuit C17, a 1-bit full adder, a 3-bit Ripple Carry Adder, and the ISCAS-85 Benchmark Circuit 74182) have also been evaluated.

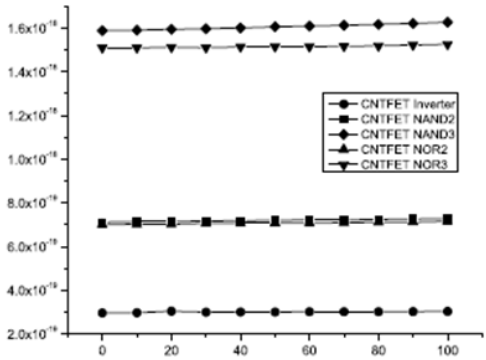


Figure 3.23: Power delay product (PDP) of 32 nm carbon nanotube field effect transistor (CNTFET) logic gates vs. temperature.

CNTFET threshold voltage check add formula

CNTFETs utilize semiconducting SWCNTs to assemble electronic devices [17]. A SWCNT consists of one cylinder only, and the simple manufacturing process of this device makes it very promising .A SWCNT can act as either a conductor or a semiconductor, depending on the angle of the atom arrangement along the tube. This is referred to as the chirality vector and is represented by the integer pair (n, m).A simple method to determine if a CNT is metallic or semiconducting is to consider its indexes (n, m): the nanotube is metallic if n = m or n-m = 3i, where i is an integer. Otherwise, the tube is semiconducting. The diameter of the CNT can be calculated based on the foll

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \quad (1)$$

where a 0 = 0.142 nm is the interatomic distance between each carbon atom and its neighbor. The threshold voltage is defined as the voltage required turning ON transistor. The threshold voltage

of the intrinsic CNT channel can be approximated to the first order as the half band gap that is an inverse function of the diameter i.e.

$$V_{th} \approx \frac{Eg}{2e} = \frac{\sqrt{3}}{3}\frac{aV\pi}{eD_{CNT}} \quad (2)$$

where a=2.49 angstrom is carbon to carbon atom distance, and Vπ = 3.033 eV is the carbon π–π bond energy in the tight bonding model, eis the unit electron charge, and DCNT is the CNT diameter. As DCNTof a (19, 0) CNT is 1.487 nm, the threshold voltage of a CNTFET using (19, 0) CNTs as channels is 0.293 V from Eq. (26). As the chirality vector changes, the threshold voltage of the CNTFET will also change. Assume that m in the chirality vector is always zero, and then the ratio of the threshold voltages of two CNTFETs with different chirality vectors is given as:

$$\frac{V_{th1}}{V_{th2}} = \frac{D_{CNT2}}{D_{CNT1}} = \frac{n_2}{n_1} \quad (3)$$

Equation (27) shows that the threshold voltage of a CNTFET is inversely proportional to the chirality vector of the CNT. For example, the threshold voltage of a CNTFET using (13,0) CNTs is 0.428 V, compared to a (19,0) CNTFET with a threshold voltage of 0.293 V.

TERNARY QUANTUM LOGIC GATES

Most recent upcoming technology is based on quantum logic. Ternary logic gates in quantum logic are also referred to as Qudits or Qurtit. Qudits are made up of controlled particles and the means of control (e.g. devices that trap particles and switch them from one state to another).

In multi-valued (MV) Quantum Computing (QC), the unit of memory (information) is *qudit* (*qu*antum *di*g*it*). MV quantum logic operations manipulate qudits, which are microscopic entities such as a photon's polarization or atomic spin. Ternary logic values of 0, 1, and 2 are represented by a set of distinguishable different states of a ***qutrit*** (*qu*antum *ter*nary dig*it*)). These states can be a photon's polarizations or an elementary particle's spins. After encoding these distinguishable quantities into multiple-valued constants, qutrit states are represented by $|0\rangle$, $|1\rangle$, and $|2\rangle$, respectively.

Qudits exist in a linear superposition of states, and are characterized by a wavefunction ø . As an example ($d = 2$), it is possible to have light polarizations other than purely horizontal or vertical, such as slant 45° corresponding to the linear superposition of $ø = \frac{1}{2}\left[\sqrt{2}|0\rangle + \sqrt{2}|1\rangle\right]$. In ternary logic, the notation for the superposition is $á|0\rangle + â|1\rangle + ã|2\rangle$, where α, β, and γ are complex numbers. These intermediate states cannot be distinguished, rather a measurement will yield that the qutrit is in one of the basis states, $|0\rangle$, $|1\rangle$, or $|2\rangle$. The probability that a measurement of a qutrit yields state $|0\rangle$ is $|á|^2$, state $|1\rangle$ is $|â|^2$, and state $|2\rangle$ is $|ã|^2$. The sum of these probabilities is one. The absolute values are required since, in general, α, β and γ are complex quantities.

Pairs of qutrits are capable of representing nine distinct states, $|0\,\rangle$, $|0\,\rangle$, $|0\,\rangle$, $|0\,\rangle$, $|1\,\rangle$, $|1\,\rangle$, $|1\,\rangle$, $|1\,\rangle$, and $|2\,\rangle$, as well as all possible superpositions of the states. This property may be mathematically described using the tensor product operation ⊗ [1]. The tensor product of

matrices is defined as follows:

$$\begin{bmatrix} a & b \\ c & d \end{bmatrix} \otimes \begin{bmatrix} x & y \\ z & v \end{bmatrix} = \begin{bmatrix} a\begin{bmatrix} x & y \\ z & v \end{bmatrix} & b\begin{bmatrix} x & y \\ z & v \end{bmatrix} \\ c\begin{bmatrix} x & y \\ z & v \end{bmatrix} & d\begin{bmatrix} x & y \\ z & v \end{bmatrix} \end{bmatrix} = \begin{bmatrix} ax & ay & bx & by \\ az & av & bz & bv \\ cx & cy & dx & dy \\ cz & cv & dz & dv \end{bmatrix}$$

As an example, consider two qutrits with $\psi_1 = \alpha_1|0\rangle + \beta_1|1\rangle + \gamma_1|2\rangle$ and $\psi_2 = \alpha_2|0\rangle + \beta_2|1\rangle + \gamma_2|2\rangle$. When the two qutrits are considered to represent a state, that state ψ_{12} is the superposition of all possible combinations of the original qutrits, where

$$\psi_{12} = \psi_1 \otimes \psi_2 = \alpha_1\alpha_2|00\rangle + \alpha_1\beta_2|01\rangle + \alpha_1\gamma_2|02\rangle + \beta_1\alpha_2|10\rangle + \beta_1\beta_2|11\rangle + \beta_1\gamma_2|12\rangle + \gamma_1\alpha_2|20\rangle + \gamma_1\beta_2|21\rangle + \gamma_1\gamma_2|22\rangle$$

Superposition property allows qubit states to grow much faster in dimension than classical bits, and qudits faster than qubits [18]. An output of a gate is obtained by multiplying the unitary matrix of this gate by the vector of Hilbert space corresponding to this gate's input state. A resultant unitary matrix of arbitrary quantum circuit is created by matrix or tensor multiplications of composing subcircuits. These all contribute to difficulty in understanding the concepts of quantum computing and creating efficient analysis, simulation, verification and synthesis algorithms.

Some Ternary Permutation Gates

Any unitary matrix represents a quantum gate. If a unitary matrix has only one 1 in every column and the remaining elements are 0, then such a matrix is called a permutation matrix. A quantum gate represented by a permutation matrix is called a permutation quantum gate.

Figure 3.24 shows a 2*2 ternary Feynman gate, which is the ternary counterpart of the binary Feynman gate with GF2 (Galois Field) sum replaced by GF3 sum. Here *A* is the controlling input and *B* is the controlled input. The output *P* is equal to the input *A* and the output *Q* is GF3 sum of *A* and *B*. Observe that GF3 sum is the same as modulo 3 sum. If $B = 0$, then $Q = A$ and the ternary Feynman gate acts as a copying gate. The ternary 2*2 Feynman gate is practically realizable.

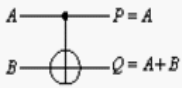


Figure 3.24:2*2 ternary Feynman gate

Gate Name	Gate Symbol with operator	Gate No. to refer in the text
Buffer	$x \to x$	0
Single-Shift	$x \to x' = x+1$	1
Dual-Shift	$x \to x'' = x+2$	2
Self-Shift	$x \to x''' = 2x$	3
Self-Single-Shift	$x \to x^{\#} = 2x+1$	4
Self-Dual-Shift	$x \to x^{\wedge} = 2x+2$	5

* Addition and multiplication are over GF3.

Fig.3.25:Ternary shift gate

Original shift gate	Mirror gate

Fig.3.26:Mirror gate

A 2*2 gate called **Generalized Ternary gate (GTG gate)** is shown in Figure 3.27 Here, input A is the controlling input and input B is the controlled input. The output P is equal to the input A. The controlling input A controls a conceptual ternary multiplexer (a conditional gate) that can be realized using quantum technology such as ion traps. If $A = 0$, then the output Q is the x shift of the input B. Similarly, if $A = 1$, then the output Q is the y shift of the input B and if $A = 2$, then the output Q is the z shift of the input B. Here shift means all ternary shift operations including the Buffer (simple quantum wire). It should note that depending on the six possible Shift gate for each of the three positions of x, y, and z, there are $6^3 = 216$ possible GTG gates. As the Conditional gate and the Shift gates are realizable in quantum technology, the GTG gate is a truly realizable ternary quantum gate.

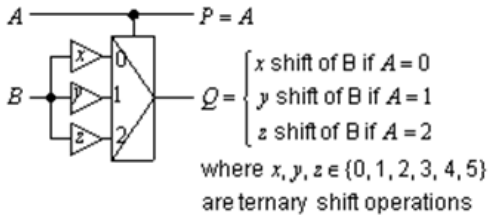


Fig. 3.27: 2*2 Generalized Ternary gates.

General Model of Synthesizing Multi-Output Ternary Functions using Cascades of GTG Gates

Realization of ternary half-adder function $C(A, B) = [0, 0, 0, 0, 0, 1, 0, 1, 1]^T$ and $S(A, B) = [0, 1, 2, 1, 2, 0, 2, 0, 1]^T$ (which is a multi-output irreversible function) using cascade of GTG gates (which is a reversible gate) is shown in Figure 3.28. Signal values at all intermediate wires are shown as maps to verify the correctness of the circuit. In this realization we assumed the following:

(1) A GTG gate can be controlled either from top or from bottom.

(2) A limited vertical wire crossing for the controlling signals of GTG gates is allowed.

(3) Constant input signals 0, 1, or 2 are added as needed to help convert the irreversible function into reversible one.

(4) Output may be realized along any primary input line or any constant input line.

(5) Each of the GTG gate form a column where the remaining lines represent quantum wires. The columns are cascaded to realize the circuit.

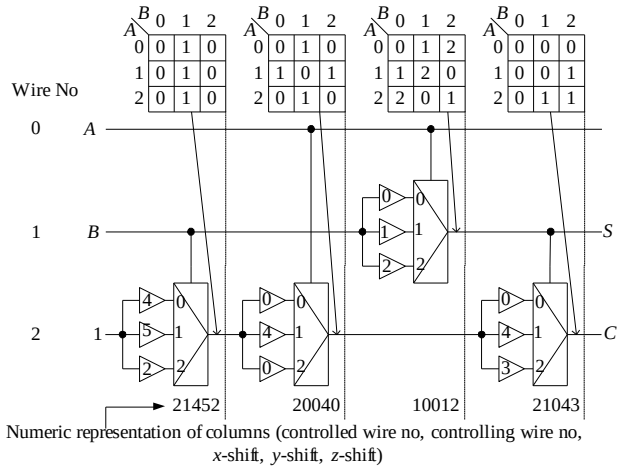


Figure 3.28: Realization of ternary half-adder function c(A,B)= $[0,0,0,0,0,1,0,1,1]^T$ and S(A,B)= $[0,1,2,1,2,0,2,0,1]^T$ using cascades of GTG gates.

By adopting this method any ternary logic function can be realized.

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