FORM 2

THE PATENT ACT 1970

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COMPLETE SPECIFICATION

(See section 10: rule 13)

1. TITLE OF INVENTION

VTI-MOSFET DEVICES

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3. PREAMBLE TO THE DESCRIPTION

COMPLETE

Following specification particularly describes the invention and the manner in which it is to be performed.

4. DESCRIPTION.

Technical field of invention:

Present invention in general relates to enhancement metal–oxide–semiconductor field-effect transistor (E-MOSFET) devices and particularly to insulated back means complimentary gate E-MOSFET devices, and its implementation in ULSI, VLSI for binary, ternary and multi-value logic circuits.

Prior art:

Complementary metal on silicon particularly enhancement type CMOS, hereinafter referred to as CMOS, comprising metal on silicon field effect transistors , hereinafter referred to as MOSFET, of 'N' and 'P' type, are extensively used in present day ULSL, VLSI circuit right from computers to a small consumer product due to it's low stand-by power losses and low voltage capability. The manufacturing technology has reduced the dimensions of MOSFET transistor means CMOS to nano meter and scaled down the size of electronic circuit. However, at present the design and implementation of CMOS is focused particularly to binary logic having two stable states. Further the capacity of binary logic circuits in modern applications especially computers, in terms of data, addressing capacity and data handling speed is limited to 2^n where 'n' is the number of bits. Due to extensive use of computers globaly there is going to be a limitation to handle extensively large data in terms of Yotta (10^{24}) or even more in coming future. Due to the advent of circuits employing Multi Value Logic (MVL) particularly Ternary system with radix as '3' having data and addressing capacity to 3^m where 3 is the radix and 'm' is number of the Trits, which has capacity to scale up future computing machine capacity many fold. Ternary computing machines, therefore, has become a main focus of present day research. However; the basic characteristics of existing CMOS devices pose multiple problems in realization of MVL circuits as regards complexity in circuit implementation and large device number, thereby posing a serious challenge.

The construction of hitherto manufactured CMOS comprises an N & P type MOSFET transistors having a drain, a source, a gate and a substrate; and have typical circuit topology wherein the substrate has to be tied to either source or drain depending on N or P type respectively to keep internal P-N junction reverse biased. In certain circuit topology the control of the ON or OFF operation requires to occur at specific threshold voltage (V_T) between the said front gate and substrate. Though a minor change in V_{TH} can be achieved by various intrinsic methods as suggested at fabrication level by varying the doping level of substrate, deep insulation layer, front gate insulator thickness; however;

biasing at other bus voltage, as required in MVL, is not possible lest substrate diode be forward biased. It is known that in enhancement type CMOS the inversion by minority carriers, in the depletion region is controlled by the voltage difference between the control gate means front gate (G_F) and substrate which is known as gate-substrate voltage (Vgs). Typically in N type MOS when Vgs is zero or negative, the region between source (N) and drain (N) has majority P carriers, thus forming a parasite NPN transistor comprising two back to back PN junctions' means diodes which blocks the flow of drain to source current I_{ds}. The substrate diodes thus create a restriction for substrate terminal connection to positive voltage with respect to source terminal, which being tied to ground or zero or negative potential. If the substrate terminal is connected to higher potential with respect to source then it results in substrate current flowing to source, which is prohibited for normal functioning of the said device. Thus the substrate cannot be biased to higher voltage, means gate operating voltage V_T is tied to source voltage. Heretofore no extrinsic method has been suggested to bias the substrate to any other circuit voltage whereby adjustment of the $\mathbf{V_T}$ voltage would be possible with respect to substrate bias voltage.

To lower stand-by power losses, CMOS have been extensively used in almost all logic circuit applications comprising complimentary N-MOSFET and P-MOSFET in series. Another device in prior art known as depletion CMOS comprises the channel region doped with N impurities for N-type and P impurities for P-type D-MOSFET, wherein the device is normally in ON state and goes in OFF state when gate is reverse bias with respect to substrate; however these devices do find applications in digital switching circuits except as resistance, constant current source etc. Still another device in prior art known as Double Gate MOSFET or DGMOSFET comprising a channel region, being intrinsic means void of impurities, and the said channel comprising having a drain, a source being sandwiched between two insulated gates, wherein the gate namely top means front gate and bottom means back gate work in tandem or independently with respect to source voltage; however; there devices are in communication circuit, modulating and mixing circuits.

A device under disclosure comprises a drain, a source, a control gate means front gate, hereinafter referred to as $\mathbf{G_F}$ and an insulated back gate means complimentary gate, hereinafter referred to as $\mathbf{G_C}$, disposed on the substrate, and the said device, comprising **V**ariable **T**hreshold **I**nsulate **C**omplimentary **G**ate MOSFET means, abbreviated as, VTICG MOSFET means in short referred to as VTI-MOSFET device, exhibits a distinguishing feature of having a variable threshold voltage owing to the choice of voltage biasing of Gc with respect to $G_{F.}$; whereas MOSFET in prior art are not suitable. The said device comprises two polarities configuration such as N-type and P-type. N-type configuration

becomes ON whenever voltage (Vf) applied to G_F is sufficiently positive than complimentary gate voltage Vc applied to $G_{C;}$ whereas in P-type configuration becomes ON whenever voltage (Vf) applied to complimentary gate G_F is sufficiently negative than voltage Vc ; further being independent of drain and source voltages. Such unique characteristic is achieved by connecting G_F to a voltage, may be fixed or variable within the circuit topology; whereas the G_C be connected to any voltage, may be fixed or variable within the circuit topology, thereby achieving variable threshold voltage characteristic. Furthermore, the device VTI-MOSFET under disclosure, be it a N-type or P-type, a complimentary characteristic achieved by interchanging drain and source terminals along with interchanging G_C and G_F gates terminals. VTI-MOSFET device works as its compliment by suitably rearranging source, drain, front gate, complimentary gate terminals. Thus the fabrication of circuit, comprising only one type of device, requiring single type of doping, can tremendously simplify VTI_MOSFET devices requiring single doping as against double doping as hitherto demanded in CMOS fabrication in prior art. Such unique single device topology renders simple fabrication process thus lowering manufacturing time and cost; and further the circuit topology rendered simplified with many added advantages.

Various methods have been suggested in research papers and patent documents:

US 3,356,858 suggested a fabrication method using pair of complimentary N-MOSFET and P-MOSFET transistors to obtain low ON state current means losses in digital circuits wherein the switching losses are the function of circuit voltage and fixed threshold voltage.

US8,716,799 B2 suggested a MOSFET incorporating buried insulation layer in the substrate during the fabrication process to adjust the threshold voltage, however, it is suitable for conventional or Sub-1 volt binary logic circuit topology or communication circuits only.

US694129B2 suggested to incorporate double gate MOSFET comprising a hitherto referred drain and source terminals over an intrinsic region and the said intrinsic region is sandwiched between a Top means front gate and a Bottom means back gate, both being their mirror image, such that the each of the said gate operates independently or jointly; and the threshold voltage is with respect to source voltage for N-type device; and is suitable for communication circuits, mixing, modulation.

A need is therefore felt to have a said VTI-MOSFET device topology under disclosure, having low stand-by power loss and further dispensing with inherent restriction on substrate voltage of hitherto MOSFET devices and a freedom of selection of substrate voltages means insulated substrate voltage means complimentary gate voltage (Vc) as well as front gate voltage means front gate voltage (Vf) for controlling the switching operation in digital circuit, be it a binary, ternary or multi value logic (MVL), rendered possible and thereby enhancing the possibility of reduction in component count and circuit simplicity to reduce switching losses and reduce propagation delays, reduce stand-by circuit losses thereby and improving related circuit performance factors and further eliminating complimentary MOSFET (CMOS) configuration only by a single device VTI-MOSFET topology to enhance switching speed, minimize process time, and fabrication cost.

Object:

1. Primary objective of the present invention is to dielectrically insulate the substrate and to provide insulated back gate means complimentary gate.
2. Another objective of the present invention is to dispense with complimentary MOSFET topology by single device hereinafter referred to VTI-MOSFET topology, may be it N-type or P-type.
3. Another objective of the present invention is to incorporate a variable threshold voltage (V_{TH}) capability means input voltage between front gate and insulated complimentary gate only which being biased to a suitable voltage, be it fixed or variable, within circuit voltage limits.

4. Another objective of the present invention is to replace conventional CMOS topology preferably by four-terminal N-type VTI-MOSFET to enhance circuit switching speed due to its inherent higher charge mobility.
5. Another objective of the present invention is to render low stand-by and short circuit losses during switching operation by optimizing threshold voltage by suitable bias voltage.
6. Another objective of the present invention is to preserve normal operation and performance of enhancement MOSFET device of prior art.
7. Another objective of the present invention is to provide a five terminal VTI-MOSFET device embodiment wherein conventional direct substrate terminal disposed on the substrate layer to render flexibility in circuit applications in MOSFET memory circuits.

8. Another objective of the present invention is to minimize process time and fabrication cost by employing single device (VTI-MOSFET) fabrication as against hitherto employed CMOS fabrication involving multiple doping process.
9. Another objective of the present invention is to facilitate the manufacturing, fabrication of proposed embodiment in the present state-of-the-art MOSFET manufacturing and fabrication process.
10. Another objective of the present invention is to facilitate flexibility in Binary, Ternary and MVL circuits MOSFET logic designs, as against binary logic circuit using CMOS in prior art.
11. Another objective of the present invention is to simplify the design of transmission gate (TG).
12. Another objective of the present invention is to simplify the design of all conventional Binary logic circuits, MVL including Ternary logic gates, Arithmetic & Logic Unit (ALU), combination logic circuit, sequential logic circuit, memory circuits, memory and other related circuits.

Further objects and features can be readily understood by any person skilled in the art by referring to the detailed description and appended claims of the invention.

STATEMENT:

Present invention under disclosure provides a four terminal MOSFET, hereinafter referred to as VTI-MOSFET, be an enhancement N-type and P-type polarities, and working exclusively either in N-type in conjunction with N-type complimentary or P-type and P-type complimentary or be in complementary N-type and P-type formation and each is having a drain, a source, a control gate means front gate (G_F) and proposed insulated back-gate means complimentary gate (G_C) thereby building a four terminal device, and according to one of the aspects of the present disclosure, a typical device may comprise an SOI wafer or any other fabrication processes, comprising a semiconductor substrate suitably doped with impurity; a gate means front gate means G_F, which is disposed on the insulation disposed over semiconductor substrate layer; a source region and a drain region, which is disposed in the semiconductor layer and on opposite side of the said G_F stack; a channel region, which is disposed in the semiconductor layer and sandwiched between the source region and the drain region, and further the said device comprises a back gate means complimentary gate G_C being disposed on the top of insulation layer, and the insulation layer being disposed on the top of the said semiconductor substrate layer and wherein

G_C terminal comprises suitable conducting contact material, may be in the form of poly-silicon or any other suitable material for further electric connection; thus the direct path of the said substrate is substituted by capacitive path means through an insulation thereby rendering freedom to the said **G_C** connection to any suitable voltage within the circuit topology, unlike the devices in the prior art and the device under disclosure functions due to difference of voltage between said G_F and said **G_C**, which are being independent of Vss and Vdd and further said device functions as its complimentary device by interchanging drain and source terminals; and by interchanging G_F and **G_C** connections concurrently, thereby said N-type device functions like said P-type device and vice the versa, and due to such unique characteristic, conventional CMOS topology in prior art be replaced exclusively either by N-type or P-type MOSFET with their said complimentary device configurations, and thereby hitherto implemented CMOS fabrication wherein N-type and P-type topology be dispensed with and further switching characteristic of the said devices be controlled externally by suitably biasing the **G_F** or **G_C** rendering many more advantages over device in prior art and further in another preferred embodiment of the said device, a fifth terminal from the substrate be made available for further simplifying circuit and semiconductor memory.

Other objects, features and advantages will become apparent from detail description and appended claims to those skilled in art.

BRIEF DESCRIPTION OF DRAWING:

Sheet 9/1: Figure A, Figure-B and Figure C schematically show cross-sectional views of prior art enhancement N-type CMOS, Depletion N-type CMOS, and Double insulated gate N-type MOSFET devices respectively.

Sheet 9/2: Figure 1A and Figure 1B schematically show cross-sectional views of N-type and P-type VTI-MOSFET depicting **G_C** respectively according to present disclosure.

Sheet 9/3: Figure 2A and Figure 2B schematically show cross-sectional views of 4-terminal N-type and P-type VTI-MOSFET with **G_C** respectively disposed on the substrate in SOI in planar fabrication according to present disclosure.

Sheet 9/4: Figure 3A and Figure 3B schematically shows cross-sectional views of 5-terminal N-type and P-type VTI-MOSFET in planer fabrication process, depicting various external connections including **G_C** and conventional back gate

disposed on formed layers of the substrate respectively according to present disclosure.
Sheet 9/5: Figure 4A, Figure 4B and Figure4C show device functioning/operation under different $\mathbf{G_F}$ and $\mathbf{G_C}$ bias voltage conditions.
Sheet 9/6: Figure 5A and Figure 5B show circuit symbol of the devices under disclosure. Figures 6A, Figure 6B show inverter means NOT gate circuit topology implementation using prior art CMOS, proposed N-type & P-type VTI-MOSFET.
Sheet 9/7: Figures 7A, 7B and 7C show input/output characteristics of prior art CMOS and Figures 8A, 8B and 8C show input/output characteristics of N-type and P-type VTI-MOSFET under disclosure under a suitable bias voltages.
Sheet 9/8: Figures 9A schematically shows cross-sectional views of two N-type VTI-MOSFET, disposed in a complimentary form, with their connection for inverter means NOT gate topology. Figures 9B shows inverter means NOT gate circuit topology implementation using two N-type VTI-MOSFET according to present disclosure.
Sheet 9/9: Figures 10A schematically shows a Ternary logic inverter means TNOT gate circuit topology implementation by using proposed N-type and P-type VTI-MOSFET according to present disclosure. Figures 10B schematically shows a Ternary logic TNOT gate circuit topology implementation comprising N-type VTI-MOSFETs devices. Figures 10C and Figure 10D show input/output relations of Ternary logic TNOT Gate circuit configuration respectively.

In order and the manner in which the above-cited and other advantages and objects of the invention are obtained, a more particular description of the invention briefly described above will be referred to, which are illustrated in the appended drawing. Understanding that these drawing depict only typical embodiment of the invention and therefore not to be considered limiting on its scope, the invention will be described with additional specificity and details through the use of the accompanying drawing.

Detailed description:

Illustrated in Figure A is an N-type enhancement MOSFET device comprising front gate block insulated from semiconductor having P type impurities; a source region and a drain region is formed in the said substrate; and a substrate terminal is brought out. Figure B is an N-type depletion MOSFET device comprising front gate block insulated from semiconductor having N type impurities; the said region is formed in the well of a P-type substrate; a source region and a drain region is formed in the said N- type substrate; and terminal is brought out from P-type a substrate. Figure C is an N-

type double gate MOSFET device comprising front gate block insulated from intrinsic semiconductor; a bottom gate block is formed insulated from the said intrinsic region and aligned to the said top gate means a mirrored gates, and in the said intrinsic region sandwiched between the said double gates a source region and a drain region is formed.

Illustrated in Figure 1A is a cross section of silicon wafer comprising N-type VTI-MOSFET device 10 disclosed in the present invention, which comprises a substrate or body 11 of semiconductor material, such as silicon. The silicon body 11 is doped in conventional manner with suitable P-type impurities. Also formed in the silicon body 11 are N-type, preferably heavily doped, diffused regions 13 and 14, provided with suitable contact material formed such that the metal is overlaps the inside surface of the diffused region 13 and 14 and leads are attached to respective connections 13' and 14' and extended over the upper surface 12 of said N-type VTI-MOSFET device respectively. An insulation layer 16, having certain thickness, preferably of silicon dioxide or any other suitable material, is grown on the body surface 12 by established method and is sandwiched or located between in the part of source 13 and drain 14. A metallic gate 15, preferably of poly silicon or other suitable material is disposed in contact with portion of the insulating material surface 17 such that certain portion of the insulation layer 16 and associated metallic contact 15 overlap part of the diffused surfaces 13 and 14 so as form a region 11'; and lead 15' is attached to the gate metallic surface 15. Region 18 is formed below the surface 12' of silicon body 11 preferably heavily doped in conventional manners with suitable P-type impurities. An insulation layer 17, preferably of silicon dioxide or any other suitable material, having certain thickness, is grown on the body surface 12' and disposed over doped region 18 by established method. A metallic layer 19, preferably of poly silicon or other suitable material is disposed in contact with the insulating material surface 17 and lead 19' is attached to the said complimentary gate metallic surface.

Illustrated in Figure 1B is a cross section of silicon wafer comprising P-type VTI-MOSFET device 20 disclosed in the present invention, which comprises a substrate or body 11 of semiconductor material, such as silicon. The silicon body 11 is doped in conventional manner with suitable P-type impurities. A well 21 of N-doped material is formed within the P-type substrate body 11. In the silicon well 21 also formed are P-type, preferably heavily doped, diffused regions 23 and 24, provided with suitable contact material formed preferably by evaporation technique such that the metal is overlaps the inside surface of the diffused region 23 and 24 so as to form a region 21' and leads are attached to respective connections 23' and 24' and extended over the upper surface 22 thus forming source 23' and drain 24' terminals of said device respectively. An

insulation layer 16, having certain thickness, preferably of silicon dioxide or any other suitable material, is grown on the body surface 22 by established method and is sandwiched or located between in the part of source 23 and drain 24. A metallic gate 25, preferably of poly silicon or other suitable material is disposed in contact with portion of the insulating material surface 16 such that certain portion of the insulation layer 26 and associated metallic contact 25 overlap part of the diffused surfaces 23 and 24 so as to form a region 21' and lead 25' is attached to the gate metallic surface. Region 28 is formed below the surface 22' of silicon body 21 preferably heavily doped in conventional manner with suitable N-type impurities. An insulation layer 27, preferably of silicon dioxide or any other suitable material, having certain thickness, is grown on the body surface 22' and disposed over doped region 28 by established method. A metallic complimentary gate 29, preferably of poly silicon or other suitable material is disposed in contact with the insulating material surface 27 and lead 29' is attached to the complimentary gate metallic surface.

Illustrated in Figure 2A is a cross section of SOI wafer comprising planar N-type VTI-MOSFET device 30 disclosed in the present invention, which comprises a substrate or body 11 of semiconductor material, such as silicon. The silicon body 11 is doped in conventional manner with suitable P-type impurities. Also formed in the silicon body 11 are N-type, preferably heavily doped, diffused regions 13 and 14, provided with suitable contact material formed preferably by evaporation technique such that the metal is overlaps the inside surface of the diffused region 13 and 14 and leads are attached to respective connections 13' and 14' and extended over the upper surface 12 thus forming source 13' and drain 14' terminals of said planar N-type VTI-MOSFET device respectively. An insulation layer 37, having certain thickness, preferably of silicon dioxide or any other suitable material, is grown on the body surface 12 by established method and is sandwiched or located between in the part of source 13 and drain 14. A metallic gate 15, preferably of poly silicon or other suitable material is disposed in contact with portion of the insulating material surface 17 such that certain portion of the insulation layer 16 and associated metallic contact 15 overlap part of the diffused surfaces 13 and 14 so as form a region 11' and lead 15' is attached to the gate metallic surface 15. Region 38 is formed below the surface 12 of silicon body 11 preferably heavily doped in conventional manner with suitable P-type impurities. An insulation layer 37, preferably of silicon dioxide or any other suitable material, having certain thickness, is grown on the body surface 12 and disposed over doped region 38 by established method. A metallic layer complimentary gate 39, preferably of poly silicon or other suitable material is disposed in contact

with the insulating material surface 37 and lead 39' is attached to the complimentary gate metallic surface.

Illustrated in Figure 2B is a cross section of SOI wafer comprising planar P-type VTI-MOSFET device 40 disclosed in the present invention, which comprises a substrate or body 11 of semiconductor material, such as silicon. The silicon body 11 is doped in conventional manner with suitable P-type impurities. A well 21 of N-doped material is formed within the P-type substrate body 11. In the silicon well 21 also formed are P-type, preferably heavily doped, diffused regions 23 and 24, provided with suitable contact material formed preferably by evaporation technique such that the metal is overlaps the inside surface of the diffused region 23 and 24 so as to form a region 21' and leads are attached to respective connections 23' and 24' and extended over the upper surface 22 thus forming source 23' and drain 24' terminals of said device respectively. An insulation layer 16, having certain thickness, preferably of silicon dioxide or any other suitable material, is grown on the body surface 22 by established method and is sandwiched or located between in the part of source 23 and drain 24. A metallic gate 25, preferably of poly silicon or other suitable material is disposed in contact with portion of the insulating material surface 16 such that certain portion of the insulation layer 26 and associated metallic contact 25 overlap part of the diffused surfaces 23 and 24 so as to form a region 21' and lead 25' is attached to the gate metallic surface. Region 48 is formed below the surface 22 of silicon body 21 preferably heavily doped in conventional manner with suitable N-type impurities. An insulation layer 47, preferably of silicon dioxide or any other suitable material, having certain thickness, is grown on the body surface 22 and disposed over doped region 48 by established method. A metallic complimentary gate 49, preferably of poly silicon or other suitable material is disposed in contact with the insulating material surface 47 and lead 49' is attached to the complimentary gate metallic surface.

Illustrated in Figure 3A is a cross section of SOI wafer comprising planar N-type VTI-MOSFET device 50 disclosed in the present invention, which comprises a substrate or body 11 of semiconductor material, such as silicon. The silicon body 11 is doped in conventional manner with suitable P-type impurities. Also formed in the silicon body 11 are N-type, preferably heavily doped, diffused regions 13 and 14, provided with suitable contact material formed preferably by evaporation technique such that the metal is overlaps the inside surface of the diffused region 13 and 14 and leads are attached to respective connections 13' and 14' and extended over the upper surface 12 thus forming source 13' and drain 14' terminals of said planar N-type VTI-MOSFET device respectively. An insulation layer 37, having certain thickness, preferably of silicon dioxide or any other suitable material, is grown

on the body surface 12 by established method and is sandwiched or located between in the part of source 13 and drain 14. A metallic gate 15, preferably of poly silicon or other suitable material is disposed in contact with portion of the insulating material surface 17 such that certain portion of the insulation layer 16 and associated metallic contact 15 overlap part of the diffused surfaces 13 and 14 so as form a region 11' and lead 15' is attached to the gate metallic surface 15. Region 38 below the surface 12 of silicon body 11 preferably heavily doped in conventional manner with suitable P-type impurities. An insulation layer 37, preferably of silicon dioxide or any other suitable material, having certain thickness, is grown on the body surface 12 and disposed over doped region 38 by established method. A metallic complimentary gate 39, preferably of poly silicon or other suitable material is disposed in contact with the insulating material surface 37 and lead 39' is attached to the complimentary gate metallic surface and a region 50 is formed below the surface 12 of silicon body 11 preferably heavily doped in conventional manner with suitable P-type impurities. A lead 51' is attached to the substrate region 50.

Illustrated in Figure 3B is a cross section of SOI wafer comprising planar P-type VTI-MOSFET device 60 disclosed in the present invention, which comprises a substrate or body 11 of semiconductor material, such as silicon. The silicon body 11 is doped in conventional manner with suitable P-type impurities. A well 21 of N-doped material is formed within the P-type substrate body 11. In the silicon well 21 also formed are P-type, preferably heavily doped, diffused regions 23 and 24, provided with suitable contact material formed preferably by evaporation technique such that the metal is overlaps the inside surface of the diffused region 23 and 24 so as to form a region 21' and leads are attached to respective connections 23' and 24' and extended over the upper surface 22 thus forming source 23' and drain 24' terminals of said device respectively. An insulation layer 16, having certain thickness, preferably of silicon dioxide or any other suitable material, is grown on the body surface 22 by established method and is sandwiched or located between in the part of source 23 and drain 24. A metallic gate 25, preferably of poly silicon or other suitable material is disposed in contact with portion of the insulating material surface 16 such that certain portion of the insulation layer 26 and associated metallic contact 25 overlap part of the diffused surfaces 23 and 24 so as to form a region 21' and lead 25' is attached to the gate metallic surface. Region 48 below the surface 22 of silicon body 21 preferably heavily doped in conventional manner with suitable N-type impurities. An insulation layer 47, preferably of silicon dioxide or any other suitable material, having certain thickness, is grown on the body surface 22 and disposed over doped region 48 by established method. A metallic back gate 49, preferably of poly silicon or other suitable material is disposed in contact with

the insulating material surface 47 and lead 49' is attached to the complimentary gate metallic surface and a region 60 is formed below the surface 22 of silicon body 21 preferably heavily doped in conventional manner with suitable N-type impurities. A lead 61' is attached to the substrate region 60.

Figures 4A, 4B and 4C show cross section of N-type VTI-MOSFET 70 having certain thickness comprising heavily N-doped drain 13, heavily N-doped source 14, front gate 15, P-doped substrate 11, insulation 16 sandwiched between 15 and 16, insulated back gate 19 and insulation 17 sandwiched between 11 and 19. Gate 15 and insulation 16 is partly overlapping drain 13 and source 14. When drain 13 and source 14 terminals are connected to each other and grounded. Voltage difference between G_F voltage (Vfg) and complimentary gate G_C voltage (Vcg) is Vfg-Vcg. When (Vfg-Vcg)<=0 then the holes in substrate 11 occupy the substrate entirely. Depletion regions 11' are formed only around drain 13 and source 14. A parasite NPN transistor or two back to back n-p junctions are formed thereby blocking conduction path between 13 and 14. Referring to Figure 4B, when (Vfg-Vcg)>0 means slightly positive but less than threshold voltage Vth then the holes in substrate 11 are repelled by the front gate and electrons migrate to P impurity substrate thus forming a depletion region 11' below the insulation 16 and between drain 13 and source14 and this region is also referred to as channel region and the device remains in OFF state. Referring to Figure 4C, when (Vfg-Vcg)>0 means slightly positive than threshold voltage Vth then the electrons from heavily doped regions of drain 13 and source 14 are attracted means migrated by field effect in the depletion region 11' and inversion of carriers, means P-type impurity replaced by N-type impurity, takes place in the said channel region means thereby a conducting path without junctions is formed between drain 13 and source 14 and the device goes in to ON state. In the process when Vfg > Vcg, means Vcg is more negative than Vfg, the negative field line due to Vcg field passes through the insulation 17 and attract P-doped impurities in substrate 11 thereby attracting holes also from the region 11' means field of Vcg working in conjunction means complimentary to field of Vfg means additive and further the insulating layer 17 does not allow for the conduction path hitherto appearing in prior art substrate and source, thus subsequently eliminating the restriction of back gate voltage connection in circuit topology.

For N-type VTI-MOSFET

For OFF state (Vfg-Vcg) < Vth ……..(1)
For ON state Vfg-Vcg=> Vth ……..(2)
And for complimentary operation
For OFF state (Vcg-Vfg) > Vth ……..(3)
For ON state Vcg-Vfg=< Vth ……..(4)

where voltages are with respect to source voltage.

Similarly for P-type VTI-MOSFET:

For OFF state (Vcg-Vfg) < Vth ……..(5)

For ON state Vcg-Vfg=> Vth ……..(6)

And for complimentary operation

For OFF state (Vcg-Vfg) > Vth ……..(7)

For ON state Vcg-Vfg=< Vth ……..(8)

where voltages are with respect to source voltage.

Equation 1 through 4 show that for ON or OFF state depends on the difference between Vfg and Vcg means G_F and G_C biasing voltage, means variable threshold voltage, means absolute Vfg applied to G_F varies as per the biasing voltage Vcg and similarly by inverting Vfg and Vcg the device functions as its complementary means N-type VTI-MOSFET also functions like its complimentary P-type VTI-MOSFET by inverting G_F anf G_C and vice the versa. This shows that complimentary devices as demanded in prior art be dispensed with singular means same type of devices, means either N-type or P-type VTI-MOSFET devices, for building low on state logic operation as hitherto necessarily required in the prior art for implementation of CMOS-FETs logic topology.

Figure 5A shows N-type VTI-MOSFET device symbol 80 where drain lead 13', source lead 14', front gate G_F lead 15' , complimentary gate G_C lead 19' insulated from substrate 11 with directional arrow 80' towards the substrate 11 are shown. Figure 5B shows P-type VTI-MOSFET device symbol 90 where drain lead 23', source lead 24', front gate G_F lead 25' , complimentary gate G_C lead 29' insulated from substrate 11 with directional arrow 90' away from the substrate 11are shown.

Figure 6A shows an inverter means NOT Gate circuit 100 comprising prior art CMOS device topology where P-MOS 102 comprises drain 73', substrate 79' connected positive supply Vdd, source 77', front gate 75'; similarly N-MOS 101 comprises source 74', substrate 72' connected negative supply Vss, drain 78' connected to 77', front gate 76' connected to 75' and further connected to front gate input (Vi) 70, drain 78' connected to source 77' and further connected to output (Vo) 71. Now referring to Figure 7A where 82 shows the input voltage to 71, 84 shows the threshold voltage level V_{TH} for 101 to conduct, 83 shows V_{TH} for 102 and Vss 81. In Figure 7B shows 85 being the voltage across 101; and 86 to be voltage across 102 with respect to input voltage 82. Shaded area 87 in Figure 7C shows the short circuit current duration equivalent to power loss during switching transition of devices 111 and 112 with respect to input voltage (82) transition. Figure 6B shows a NOT Gate circuit 110

for said VTI-MOSFET topology where P-type device 112 comprises drain 23'connected positive supply Vdd, , G_C 29' connected to biasing voltage Vcp, source 24', G_F 25'; similarly N-type VTI-MOSFET device 111 comprises source 14' connected to negative supply Vss,, G_C 19' connected to biasing voltage Vcn, drain 13' connected to 24', V_F 15' connected to 25' and further connected to input voltage (Vi) 40, drain 13' connected to source 24' and further connected to output voltage (Vo) 41. Referring to Figure 8B circuit 115 shows input voltage 82 to 41, 94 shows the biasing voltage and threshold voltage level V_{TH} for VTI-MOSFET N-type device 111 to conduct, 93 shows the biasing voltage and voltage level V_{TH} for device 112 to conduct and Vss 81. In Figure 8B shows 95 being the voltage across 111 and 96 to be voltage across 112 with respect to input voltage (Vi) 40. Shaded area 97 in Figure 8C shows the short circuit current duration during switching transition of devices 111 and 112 with respect to input voltage (82) transition, equivalent to power loss. The comparison of area 87 for prior art CMOS 'NOT' gate and area 97 for devices VTI-MOSFET shows that area 97 is less than area 87, meaning thereby that the short circuit losses in the devices under disclosure not only has lesser short circuit losses than prior art devices but threshold voltage level can also be controlled by external means.

Illustrated in Figure 9A is a cross section of SOI wafer comprising two planar N-type VTI-MOSFET devices and as shown in schematic diagram in Figure 9B comprising device 30 and device 30', having been isolated by layer 55, where device 30' source 34' connected to Vdd and drain 33' connected to drain 13' of device 30, G_F 35' connected to Vdd and complimentary gate G_C 39' connected to G_F 15' of device 30 means thus being in complimentary configuration; the complimentary gate G_C 19' of device 30 connected to source 14' Vss; front gate V_F 15' of device 30 connected to complimentary gate 39' of device 30' and further connected to input 50 (Vg); drain 13' of device 30 connected to source 34' of device 30' and further connected to output 51 (Vo); front gate G_F 35' connected to drain 33' of device 30' and further connected to Vdd thus forming an binary inverter or NOT gate configuration. When input voltage Vg is low then voltage between 19' and 15' ($V_C = V_F$) is zero and device 30 is OFF whereas voltage between 35' and 39' ($V_F > V_C$) is higher than threshold voltage and device 30' is ON , output 51(Vo) is HIGH; when input voltage Vg is HIGH then voltage between 19' and 15' ($V_F > V_C$) is higher than threshold voltage and device 30 is ON whereas voltage between 35' and 39' ($V_F = V_C$) is zero and device 30' is OFF , output 51(Vo) is LOW and in this manner inverter means NOT logic is achieved.

Illustrated in Figure 10A is a schematic diagram of Ternary Inverter means TNOT gate comprising N-type and P-type VTI-MOSFET devices (Figure

3A and 3B) comprising P-type 137, 138 devices and N-type 136, 139 devices; where device 137, drain 23' connected to +V (Vdd) 152, source 24' connected to drain 13' of device 136 wherein source 14' connected to negative voltage 150 (Vss), G_C 29' and G_C 19' are connected to ground 151 (0 volts Gnd), G_F 25' and G_F 15' connected to input voltage Vg 140'; device 138, G_F 125' connected to input voltage Vg 140', G_C 129' connected to Vdd 152, drain 125' connected to output 141', source 124' connected to drain 113'; device 139, drain 113' connected to source 124', source 114' connected to ground 151, G_C 119' connected to –V source 150, G_F 115' connected to input voltage Vg 140'. Figure 10C shows the ternary input voltage where level '-1' denoted by 101, level '0' denoted by 102 and level '+1' denoted by 103; Figure 10D shows the ternary output voltage where level '-1' denoted by 201, level '0' denoted by 202 and level '+1' denoted by 203;when Vg is 101 means LOW then at device 137 is ON as G_F 25' voltage is negative with respect to G_C 29'; device 136 is OFF as G_F 15' voltage is negative with respect to G_C 19'; device 138 is ON as G_F 125' voltage is negative with respect to G_C 129', device 139 is OFF as G_F 115' voltage is equal to G_C 119'; means voltage at 141' is at level 203 means HIGH; when Vg is 102 means ZERO level then at device 137 is OFF as G_F 25' voltage is equal to G_C 29'; device 136 is OFF as G_F 15' voltage is equal to G_C 29'; device 138 is ON as G_F 125' voltage is negative with respect to G_C 129', device 136 is ON as G_F 115' voltage is positive with respect to G_C 129'; means both 138 and 139 devices are ON hence voltage at 141' is at level 201 means zero; when Vg is 103 means HIGH then at device 137 is OFF as GF 25' voltage is positive with respect to G_C 29'; device 136 is ON as G_F 15' voltage is positive with respect to G_C 29'; device 138 is OFF as G_F 125' voltage is equal to G_C 129', device 139 is ON as G_F 115' voltage is positive with respect to G_C 119'; means voltage at 141' is at level 201 means LOW; hence output voltage at 141' is inverted with respect to input voltage Vg 141' means the said circuit functions like Ternary NOT means TNOT gate.

Illustrated in Figure 10B is a schematic diagram of Ternary Inverter means TNOT gate comprising all N-type VTI-MOSFET devices (Figure 3A) comprising N-type 240, 236, 241, and 339; where device 240, source 214' connected to +V (Vdd) 152, drain 213' connected to drain 213 of device 236, G_C 229' connected to input voltage 240', G_F 215' connected to ground 151, means in complimentary configuration; device 236 source 214' connected to negative voltage 150 (Vss), G_F 219' are connected to 151 ground, G_F 215' connected to input voltage Vg 240'; device 241, G_C 319' connected to input voltage Vg 240', G_F 129' connected to +V (Vdd) 152, drain 324' connected to output 241', drain 325' connected to drain 313' of device 339 means in complimentary configuration; device 339 source 351 connected to ground 151,

G_C 319’ connected to –V (Vss) , G_F 115’ connected to input voltage Vg 140’. Figure 10C shows the ternary input voltage where level ‘-1’ denoted by 101, level ‘0’ denoted by 102 and level ‘+1’ denoted by 103; Figure 10D shows the ternary output voltage where level ‘-1’ denoted by 201, level ‘0’ denoted by 202 and level ‘+1’ denoted by 203;when Vg is 101 means LOW then at device 240 is ON as G_C 229’ voltage is negative with respect to G_F 215’; device 236 is OFF as G_F 15’ voltage is negative with respect to G_C 19’; device 241 is ON as G_F 325’ voltage is negative with respect to G_C 329’, device 339 is OFF as G_F 315’ voltage is equal to G_C 319’; means voltage at 141’ is at level 203 means HIGH; when Vg is 102 means ZERO level at device 240 is OFF as G_F 215’ voltage is equal to G_C 229’; device 236 is OFF as G_F 215’ voltage is equal to G_C 219’; device 242 is ON as G_F 325’ voltage is positive with respect to G_C 319’, device 339 is ON as G_F 315’ voltage is positive with respect to G_C 349’; means both 319 and 339 devices are ON hence voltage at 141’ is at level 201 means zero; when Vg is 103 means HIGH then at device 240 is OFF as G_F 215’ voltage is negative with respect to G_C 229’; device 236 is ON as G_F 215’ voltage is positive with respect to G_C 219’; device 240 is OFF as G_F 325’ voltage is equal to G_C 319’, device 339 is ON as G_F 315’ voltage is positive with respect to G_C 349’; means voltage at 141’ is at level 201 means LOW; hence output voltage at 141’ is inverted with respect to input voltage Vg 141’ means the said circuit functions like Ternary NOT means TNOT gate.

Additional advantages and modification will readily occur to those skilled in art. Therefore, the invention in its broader aspect is not limited to specific details and representative embodiments shown and described herein. Accordingly various modifications may be made without departing from the spirit or scope of the general invention concept as defined by the appended claims and their equivalents.

CLAIMS

We claim:-

1. A double gate MOSFET device, hereinafter referred to VTI-MOSFET device, comprising :

a semiconductor wafer which comprises a doped semiconductor substrate;
a front gate stack, which is disposed on said semiconductor layer;
a source region and a drain region, which are disposed in the semiconductor layer means substrate layer;
a channel region, which is disposed in the semiconductor layer and preferably between the source and the drain region,
wherein the VTI-MOSFET further comprises an insulated back gate means complimentary gate disposed on the doped substrate layer, and the said gate comprises an insulation layer, in the form of SiO_2 or any other suitable insulating material and further having certain thickness and area disposed on to the semiconductor substrate and be placed preferably on one side or either side of the source and the drain or any suitable surface of the substrate pertaining to the said device and a conducting material is deposited on the exposed surface of the said insulation to facilitate external connection thus forming a 4-terminal VTI-MOSFET device, under disclosure, having two insulated gates.

2. The VTI-MOSFET according to claim 1, wherein N-type device comprises P-type substrate, N-type source, N-type drain, a front gate and an insulated back gate means complimentary formed on the P-type substrate, whereas P-type device comprises N-type substrate, P-type source and P-type drain, a front gate and an insulated back gate means complimentary gate formed on the N-type substrate; and said N-type substrate preferably doped inside P-type substrate well.
3. The device according to claim 1, claim 2, having an independent doped substrate terminal and an independent said complimentary gate terminal being brought out thus forming five-terminal device.

4. The devices according to claim 1, claim 2 and claim 3, wherein the said front gate, said insulated complimentary gate be connected independently to circuit voltage rendering variable threshold voltage circuit operation for

minimization of short circuit losses and stand-by losses during switching operation.

5. The devices according to claim 1, claim 2, claim 3, and claim 4 wherein the said drain, said source, said front gate and said complimentary gate be connected independently to respective circuit voltage and further said drain and source being interchangeable; and concurrently said front gate and complimentary gate being interchangeable thus rendering device to operate as its complimentary mode without any change in manufacturing process, thus rendering the said single device topology suitable for ULSI, VLSI technology as against hitherto employed complimentary device topology.

6. The devices according to claim 1, claim 2, claim 3, claim 4 and claim 5 wherein the said device functioning also as its complimentary device, thus dispensing double device processing and thereby reducing the process time, minimizing fabrication, infrastructure and cost.

7. the devices according to claim 1, claim 2 and claim 3, wherein the said deices be manufactured with SOI, and/or fingate front gate, and said insulated complimentary gate be connected independently to circuit voltage rendering variable threshold voltage circuit operation.
8. The device as claimed in claim 1 and illustrated in Figure 1A is a cross section of silicon wafer comprising N-type VTI-MOSFET device 10 disclosed in the present invention, which comprises a substrate or body 11 of semiconductor material, such as silicon and the silicon body 11 is doped in conventional manner with suitable P-type impurities; also formed in the silicon body 11 are N-type, preferably heavily doped, diffused regions 13 and 14, provided with suitable contact material formed preferably by evaporation technique such that the metal is overlaps the inside surface of the diffused region 13 and 14 and leads are attached to respective connections 13’ and 14’ and extended over the upper surface 12 thus forming source 13’ and drain 14’ terminals of said N-type VTI-MOSFET device respectively and an insulation layer 16, having certain thickness, preferably of silicon dioxide or any other suitable material, is grown on the body surface 12 by established method and is sandwiched or located between in the part of source 13 and drain 14; a metallic gate 15, preferably of poly silicon or other suitable material is disposed in contact with portion of the insulating material surface 17 such that certain portion of the insulation layer 16 and associated metallic

contact 15 overlap part of the diffused surfaces 13 and 14 so as form a region 11' and lead 15' is attached to the gate metallic surface 15 and a region 18 is formed below the surface 12' of silicon body 11 preferably heavily doped in conventional manner with suitable P-type impurities; an insulation layer 17, preferably of silicon dioxide or any other suitable material, having certain thickness, is grown on the body surface 12' and disposed over doped region 18 by established method; a metallic layer 19, preferably of poly silicon or other suitable material is disposed in contact with the insulating material surface 17 and lead 19' is attached to the said complimentary gate metallic surface.

9. As claimed in claim 1, 8 and illustrated in Figure 1B is a cross section of silicon wafer comprising P-type VTI-MOSFET device 20 disclosed in the present invention, which comprises a substrate or body 11 of semiconductor material, such as silicon and the silicon body 11 is doped in conventional manner with suitable P-type impurities; a well 21 of N-doped material is formed within the P-type substrate body 11; and in the silicon well 21 also formed are P-type, preferably heavily doped, diffused regions 23 and 24, provided with suitable contact material formed preferably by evaporation technique such that the metal is overlaps the inside surface of the diffused region 23 and 24 so as to form a region 21' and leads are attached to respective connections 23' and 24' and extended over the upper surface 22 thus forming source 23' and drain 24' terminals of said device respectively; an insulation layer 16, having certain thickness, preferably of silicon dioxide or any other suitable material, is grown on the body surface 22 by established method and is sandwiched or located between in the part of source 23 and drain 24 and a metallic gate 25, preferably of poly silicon or other suitable material is disposed in contact with portion of the insulating material surface 16 such that certain portion of the insulation layer 26 and associated metallic contact 25 overlap part of the diffused surfaces 23 and 24 so as to form a region 21' and lead 25' is attached to the gate metallic surface. Region 28 formed below the surface 22' of silicon body 21 preferably heavily doped in conventional manners with suitable N-type impurities; an insulation layer 27, preferably of silicon dioxide or any other suitable material, having certain thickness, is grown on the body surface 22' and disposed over doped region 28 by established method and a metallic complimentary gate 29, preferably of poly silicon or other suitable material is disposed in contact with the insulating material surface 27 and lead 29' is attached to the complimentary gate metallic surface.

10. As claimed in claim 1,8,9 and illustrated in Figure 2A is a cross section of SOI wafer comprising planar N-type VTI-MOSFET device 30 disclosed in the present invention, which comprises a substrate or body 11 of semiconductor material, such as silicon and the silicon body 11 is doped in conventional manner with suitable P-type impurities; and also formed in the silicon body 11 are N-type, preferably heavily doped, diffused regions 13 and 14, provided with suitable contact material formed preferably by evaporation technique such that the metal is overlaps the inside surface of the diffused region 13 and 14 and leads are attached to respective connections 13' and 14' and extended over the upper surface 12 thus forming source 13' and drain 14' terminals of said planar N-type VTI-MOSFET device respectively; an insulation layer 37, having certain thickness, preferably of silicon dioxide or any other suitable material, is grown on the body surface 12 by established method and is sandwiched or located between in the part of source 13 and drain 14 and a metallic gate 15, preferably of poly silicon or other suitable material is disposed in contact with portion of the insulating material surface 17 such that certain portion of the insulation layer 16 and associated metallic contact 15 overlap part of the diffused surfaces 13 and 14 so as form a region 11' and lead 15' is attached to the gate metallic surface 15 and a region 38 is formed below the surface 12 of silicon body 11 preferably heavily doped in conventional manner with suitable P-type impurities and an insulation layer 37, preferably of silicon dioxide or any other suitable material, having certain thickness, is grown on the body surface 12 and disposed over doped region 38 by established method; a metallic layer complimentary gate 39, preferably of poly silicon or other suitable material is disposed in contact with the insulating material surface 37 and lead 39' is attached to the complimentary gate metallic surface.
11. As claimed in claim 1, 8, 9,10 illustrated in Figure 2B is a cross section of SOI wafer comprising planar P-type VTI-MOSFET device 40 disclosed in the present invention, which comprises a substrate or body 11 of semiconductor material, such as silicon and the silicon body 11 is doped in conventional manner with suitable P-type impurities and a well 21 of N-doped material is formed within the P-type substrate body 11; in the silicon well 21 also formed are P-type, preferably heavily doped, diffused regions 23 and 24, provided with suitable contact material formed preferably by evaporation or any suitable technique such that the metal is overlaps the inside surface of the diffused region 23 and 24 so as to form a region 21' and leads are attached to respective connections 23' and 24' and extended over the upper surface 22 thus forming source 23' and drain

24’ terminals of said device respectively and an insulation layer 16, having certain thickness, preferably of silicon dioxide or any other suitable material, is grown on the body surface 22 by established method and is sandwiched or located between in the part of source 23 and drain 24 and a metallic gate 25, preferably of poly silicon or other suitable material is disposed in contact with portion of the insulating material surface 16 such that certain portion of the insulation layer 26 and associated metallic contact 25 overlap part of the diffused surfaces 23 and 24 so as to form a region 21’ and lead 25’ is attached to the gate metallic surface; region 48 is formed below the surface 22 of silicon body 21 preferably heavily doped in conventional manner with suitable N-type impurities; an insulation layer 47, preferably of silicon dioxide or any other suitable material, having certain thickness, is grown on the body surface 22 and disposed over doped region 48 by established method; a m metallic complimentary gate 49, preferably of poly silicon or other suitable material is disposed in contact with the insulating material surface 47 and lead 49’ is attached to the complimentary gate metallic surface.

12. As claimed in claims 1, 8,9,10, 11 and illustrated in Figure 3A is a cross section of SOI wafer comprising planar N-type VTI-MOSFET device 50 disclosed in the present invention, which comprises a substrate or body 11 of semiconductor material, such as silicon; and the silicon body 11 is doped in conventional manner with suitable P-type impurities and also formed in the silicon body 11 are N-type, preferably heavily doped, diffused regions 13 and 14, provided with suitable contact material formed preferably by evaporation technique such that the metal is overlaps the inside surface of the diffused region 13 and 14 and leads are attached to respective connections 13’ and 14’ and extended over the upper surface 12 thus forming source 13’ and drain 14’ terminals of said planar N-type VTI-MOSFET device respectively and an insulation layer 37, having certain thickness, preferably of silicon dioxide or any other suitable material, is grown on the body surface 12 by established method and is sandwiched or located between in the part of source 13 and drain 14; a metallic gate 15, preferably of poly silicon or other suitable material is disposed in contact with portion of the insulating material surface 17 such that certain portion of the insulation layer 16 and associated metallic contact 15 overlap part of the diffused surfaces 13 and 14 so as form a region 11’ and lead 15’ is attached to the gate metallic surface 15 and a region 38 below the surface 12 of silicon body 11 preferably heavily doped in conventional manner with suitable P-type impurities; an

insulation layer 37, preferably of silicon dioxide or any other suitable material, having certain thickness, is grown on the body surface 12 and disposed over doped region 38 by established method and a metallic complimentary gate 39, preferably of poly silicon or other suitable material is disposed in contact with the insulating material surface 37 and lead 39' is attached to the complimentary gate metallic surface and a region 50 is formed below the surface 12 of silicon body 11 preferably heavily doped in conventional manner with suitable P-type impurities and a lead 51' is attached to the substrate region 50.

13. As claimed in claims 1, 8,9,10,11,12 and illustrated in Figure 3B is a cross section of SOI wafer comprising planar P-type VTI-MOSFET device 60 disclosed in the present invention, which comprises a substrate or body 11 of semiconductor material, such as silicon and the silicon body 11 is doped in conventional manner with suitable P-type impurities; a well 21 of N-doped material is formed within the P-type substrate body 11 and in the silicon well 21 also formed are P-type, preferably heavily doped, diffused regions 23 and 24, provided with suitable contact material formed preferably by evaporation or other suitable technique such that the metal is overlaps the inside surface of the diffused region 23 and 24 so as to form a region 21' and leads are attached to respective connections 23' and 24' and extended over the upper surface 22 thus forming source 23' and drain 24' terminals of said device respectively and an insulation layer 16, having certain thickness, preferably of silicon dioxide or any other suitable material, is grown on the body surface 22 by established method and is sandwiched or located between in the part of source 23 and drain 24. A metallic gate 25, preferably of poly silicon or other suitable material is disposed in contact with portion of the insulating material surface 16 such that certain portion of the insulation layer 26 and associated metallic contact 25 overlap part of the diffused surfaces 23 and 24 so as to form a region 21' and lead 25' is attached to the gate metallic surface and a region 48 below the surface 22 of silicon body 21 preferably heavily doped in conventional manner with suitable N-type impurities; an insulation layer 47, preferably of silicon dioxide or any other suitable material, having certain thickness, is grown on the body surface 22 and disposed over doped region 48 by established method and a metallic back gate 49, preferably of poly silicon or other suitable material is disposed in contact with the insulating material surface 47 and lead 49' is attached to the complimentary gate metallic surface and a region 60 is formed below the surface 22 of silicon body 21 preferably heavily doped in

conventional manner with suitable N-type impurities. A lead 61' is attached to the substrate region 60.

14. As claimed in claims 1, 8,9,10,11,12 , 13 and illustrated in Figures 4A, 4B and 4C show cross section of N-type VTI-MOSFET 70 having certain thickness comprising heavily N-doped drain 13, heavily N-doped source 14, front gate 15, P-doped substrate 11, insulation 16 sandwiched between 15 and 16, insulated back gate 19 and insulation 17 sandwiched between 11 and 19; gate 15 and insulation 16 is partly overlapping drain 13 and source 14 and when drain 13 and source 14 terminals are connected to each other and grounded; voltage difference between G_F voltage (Vfg) and complimentary gate G_C voltage (Vcg) is Vfg-Vcg; and when (Vfg-Vcg)<=0 then the holes in substrate 11 occupy the substrate entirely and depletion regions 11' are formed only around drain 13 and source 14 and a parasite NPN transistor or two back to back n-p junctions are formed thereby blocking conduction path between 13 and 14 and now referring to Figure 4B, when (Vfg-Vcg)>0 means slightly positive but less than threshold voltage Vth then the holes in substrate 11 are repelled by the front gate and electrons migrate to P impurity substrate thus forming a depletion region 11' below the insulation 16 and between drain 13 and source14 and this region is also referred to as channel region and the device remains in OFF state and now referring to Figure 4C, when (Vfg-Vcg)>0 means slightly positive than threshold voltage Vth then the electrons from heavily doped regions of drain 13 and source 14 are attracted means migrated by field effect in the depletion region 11' and inversion of carriers, means P-type impurity replaced by N-type impurity, takes place in the said channel region means thereby a conducting path without junctions is formed between drain 13 and source 14 and the device goes in to ON state and in the process when Vfg > Vcg, means Vcg is more negative than Vfg, the negative field line due to Vcg field passes through the insulation 17 and attract P-doped impurities in substrate 11 thereby attracting holes also from the region 11' means field of Vcg working in conjunction means complimentary to field of Vfg means additive and further the insulating layer 17 does not allow for the conduction path hitherto appearing in prior art substrate and source, thus subsequently eliminating the restriction of back gate voltage connection in circuit topology and the equation 1 through 4 show that for ON or OFF state depends on the difference between Vfg and Vcg means G_F and G_C biasing voltage, means variable threshold voltage, means absolute Vfg applied to G_F varies as per the biasing voltage Vcg and similarly by inverting Vfg and Vcg the device functions as its complementary means

N-type VTI-MOSFET also functions like its conventional complimentary P-type VTI-MOSFET by inverting G_F anf G_C and vice the versa and further shows that complimentary devices as demanded in prior art be dispensed with singular means same type of devices, means either N-type or P-type VTI-MOSFET devices, for building low on state loss logic operation as hitherto necessarily required in the prior art.

15. As claimed in claims1, 8,9,10,11,12,13,14 and illustrated in Figure 5A shows N-type VTI-MOSFET device symbol 80 where drain lead 13', source lead 14', front gate G_F lead 15' , complimentary gate G_C lead 19' insulated from substrate 11 with directional arrow 80' towards the substrate 11 are shown and Figure 5B shows P-type VTI-MOSFET device symbol 90 where drain lead 23', source lead 24', front gate G_F lead 25' , complimentary gate G_C lead 29' insulated from substrate 11 with directional arrow 90' away from the substrate 11are shown.
16. As claimed in claims 1,8,9,10,11,12,13,14,15 and illustrated in Figure 6A shows an inverter means a NOT Gate circuit 100 comprising prior art CMOS device topology where P-MOS 102 comprises drain 73', substrate 79' connected positive supply Vdd, source 77', front gate 75'; similarly N-MOS 101 comprises source 74', substrate 72' connected negative supply Vss, drain 78' connected to 77', front gate 76' connected to 75' and further connected to front gate input (Vi) 70, drain 78' connected to source 77' and further connected to output (Vo) 71 and further referring to Figure 7A where 82 shows the input voltage to 71, 84 shows the threshold voltage level V_{TH} for 101 to conduct, 83 shows V_{TH} for 102 and Vss 81. In Figure 7B shows 85 being the voltage across 101; and 86 to be voltage across 102 with respect to input voltage 82; shaded area 87 in Figure 7C shows the short circuit current duration equivalent to power loss during switching transition of devices 111 and 112 with respect to input voltage (82) transition; Figure 6B shows a NOT Gate circuit 110 for said VTI-MOSFET topology where P-type device 112 comprises drain 23'connected positive supply Vdd, , G_C 29' connected to biasing voltage Vcp, source 24', G_F 25'; similarly N-type VTI-MOSFET device 111 comprises source 14' connected to negative supply Vss, G_C 19' connected to biasing voltage Vcn, drain 13' connected to 24', V_F 15' connected to 25' and further connected to input voltage (Vi) 40, drain 13' connected to source 24' and further connected to output voltage (Vo) 41. Referring to Figure 8B circuit 115 shows input voltage 82 to 41, 94 shows the biasing voltage and threshold voltage level V_{TH} for VTI-MOSFET N-type device 111 to conduct, 93 shows the biasing voltage and voltage level V_{TH} for device 112 to conduct and Vss 81 and further Figure 8B

shows 95 being the voltage across 111 and 96 to be voltage across 112 with respect to input voltage (Vi) 40; shaded area 97 in Figure 8C shows the short circuit current duration during switching transition of devices 111 and 112 with respect to input voltage (82) transition, equivalent to power loss; the comparison of area 87 for prior art CMOS 'NOT' gate and area 97 for devices VTI-MOSFET shows that area 97 is less than area 87, meaning thereby that the short circuit losses in the devices under disclosure not only has lesser short circuit losses than prior art devices but threshold voltage level can also be controlled by external means.

17. As claimed in claims 1,8,9,10,11,12,13,14,15,16 and illustrated in Figure 9A is a cross section of SOI wafer comprising two N-type VTI-MOSFET devices and as shown in schematic diagram in Figure 9B comprising device 30 and device 30', having been isolated by layer 55, where device 30' source 34' connected to Vdd and drain 33' connected to drain 13' of device 30, G_F 35' connected to Vdd and complimentary gate G_C 39' connected to G_F 15' of device 30 means thus being in complimentary configuration; the complimentary gate G_C 19' of device 30 connected to source 14' Vss; front gate V_F 15' of device 30 connected to complimentary gate 39' of device 30' and further connected to input 50 (Vg); drain 13' of device 30 connected to source 34' of device 30' and further connected to output 51 (Vo); front gate G_F 35' connected to drain 33' of device 30' and further connected to Vdd thus forming an binary inverter or NOT gate configuration and when input voltage Vg is low means at Vss then voltage between 19' and 15' ($V_C = V_F$) is zero and device 30 is OFF whereas voltage between 35' and 39' ($V_F > V_C$) is higher than threshold voltage and device 30' is ON , output 51(Vo) is HIGH; whereas when input voltage Vg is HIGH then voltage between 19' and 15' ($V_F > V_C$) is higher than threshold voltage and device 30 is ON whereas voltage between 35' and 39' ($V_F = V_C$) is zero and device 30' is OFF , output 51(Vo) is LOW and in this manner inverter means NOT logic is achieved.
18. As claimed in claims 1, 8,9,10,11,12,13,14,15,16 and illustrated in Figure 10A is a schematic diagram of Ternary Inverter means TNOT gate comprising N-type and P-type VTI-MOSFET devices (Figure 3A and 3B) comprising P-type 137, 138 devices and N-type 136, 139 devices; where device 137, drain 23' connected to +V (Vdd) 152, source 24' connected to drain 13' of device 136 wherein source 14' connected to negative voltage 150 (Vss), G_C 29' and G_C 19' are connected to ground 151 (0 volts Gnd), G_F 25' and G_F 15' connected to input voltage Vg 140'; device 138, G_F 125' connected to input voltage Vg 140', G_C 129'

connected to Vdd 152, drain 125' connected to output 141', source 124' connected to drain 113'; device 139, drain 113' connected to source 124', source 114' connected to ground 151, G_C 119' connected to –V source 150, G_F 115' connected to input voltage Vg 140'. Figure 10C shows the ternary input voltage where level '-1' denoted by 101, level '0' denoted by 102 and level '+1' denoted by 103; Figure 10D shows the ternary output voltage where level '-1' denoted by 201, level '0' denoted by 202 and level '+1' denoted by 203;when Vg is 101 means LOW then at device 137 is ON as G_F 25' voltage is negative with respect to G_C 29'; device 136 is OFF as G_F 15' voltage is negative with respect to G_C 19'; device 138 is ON as G_F 125' voltage is negative with respect to G_C 129', device 139 is OFF as G_F 115' voltage is equal to G_C 119'; means voltage at 141' is at level 203 means HIGH; when Vg is 102 means ZERO level then at device 137 is OFF as G_F 25' voltage is equal to G_C 29'; device 136 is OFF as G_F 15' voltage is equal to G_C 29'; device 138 is ON as G_F 125' voltage is negative with respect to G_C 129', device 136 is ON as G_F 115' voltage is positive with respect to G_C 129'; means both 138 and 139 devices are ON hence voltage at 141' is at level 201 means zero; when Vg is 103 means HIGH then at device 137 is OFF as GF 25' voltage is positive with respect to G_C 29'; device 136 is ON as G_F 15' voltage is positive with respect to G_C 29'; device 138 is OFF as G_F 125' voltage is equal to G_C 129', device 139 is ON as G_F 115' voltage is positive with respect to G_C 119'; means voltage at 141' is at level 201 means LOW; hence output voltage at 141' is inverted with respect to input voltage Vg 141' means the said circuit functions like Ternary NOT means TNOT gate.

19. As claimed in claims 8,9,10,11,12,13,14,15,16 and illustrated in Figure 10B is a schematic diagram of Ternary Inverter means TNOT gate comprising all N-type VTI-MOSFET devices (Figure 3A) comprising N-type devices 240, 236, 241, and 339; where device 240, source 214' connected to +V (Vdd) 152, drain 213' connected to drain 213 of device 236, G_C 229' connected to input voltage 240', G_F 215' connected to ground 151, means in complimentary configuration; device 236 source 214' connected to negative voltage 150 (Vss), G_F 219' are connected to 151 ground, G_F 215' connected to input voltage Vg 240'; device 241, G_C 319' connected to input voltage Vg 240', G_F 129' connected to +V (Vdd) 152, drain 324' connected to output 241', drain 325' connected to drain 313' of device 339 means in complimentary configuration; device 339 source 351 connected to ground 151, G_C 319' connected to –V (Vss) , G_F 115' connected to input voltage Vg 140'. Figure 10C shows the ternary

input voltage where level '-1' denoted by 101, level '0' denoted by 102 and level '+1' denoted by 103; Figure 10D shows the ternary output voltage where level '-1' denoted by 201, level '0' denoted by 202 and level '+1' denoted by 203;when Vg is 101 means LOW then at device 240 is ON as G_C 229' voltage is negative with respect to G_F 215'; device 236 is OFF as G_F 15' voltage is negative with respect to G_C 19'; device 241 is ON as G_F 325' voltage is negative with respect to G_C 329', device 339 is OFF as G_F 315' voltage is equal to G_C 319'; means voltage at 141' is at level 203 means HIGH; when Vg is 102 means ZERO level at device 240 is OFF as G_F 215' voltage is equal to G_C 229'; device 236 is OFF as G_F 215' voltage is equal to G_C 219'; device 242 is ON as G_F 325' voltage is positive with respect to G_C 319', device 339 is ON as G_F 315' voltage is positive with respect to G_C 349'; means both 319 and 339 devices are ON hence voltage at 141' is at level 201 means zero; when Vg is 103 means HIGH then at device 240 is OFF as G_F 215' voltage is negative with respect to G_C 229'; device 236 is ON as G_F 215' voltage is positive with respect to G_C 219'; device 240 is OFF as G_F 325' voltage is equal to G_C 319', device 339 is ON as G_F 315' voltage is positive with respect to G_C 349'; means voltage at 141' is at level 201 means LOW; hence output voltage at 141' is inverted with respect to input voltage Vg 141' means the said circuit functions like Ternary NOT means TNOT gate.

Ingole Vijay Tulshiram
Ingole Indira Vijay
Ingole Ashutosh Vijay

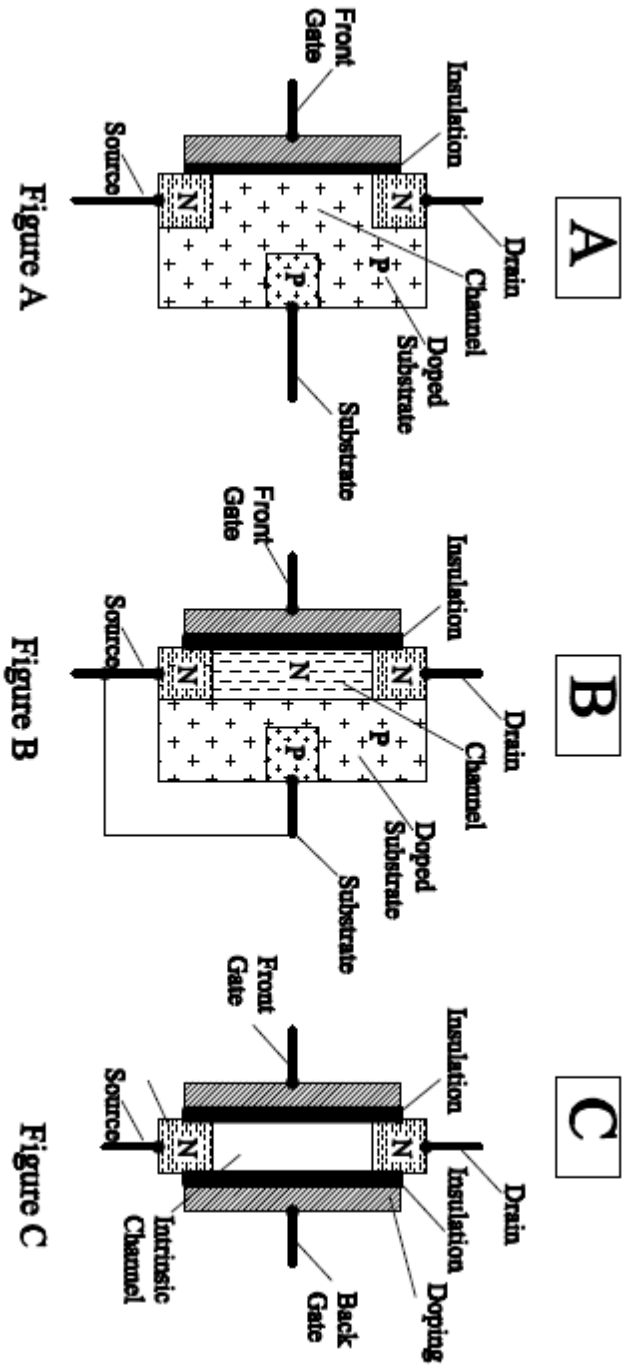


Figure A

Figure B

Figure C

Ingole Vijay Tulshiram
Ingole Indira Vijay
Ingole Ashutosh Vijay

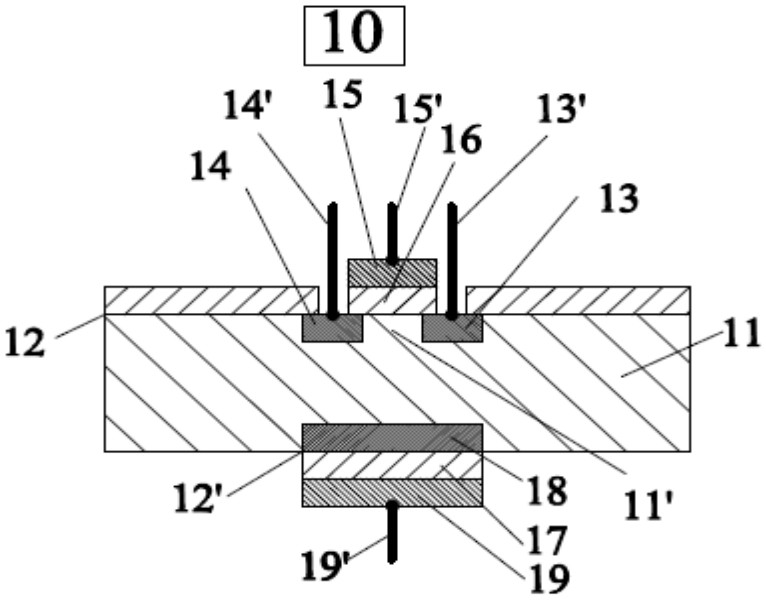


Figure 1A

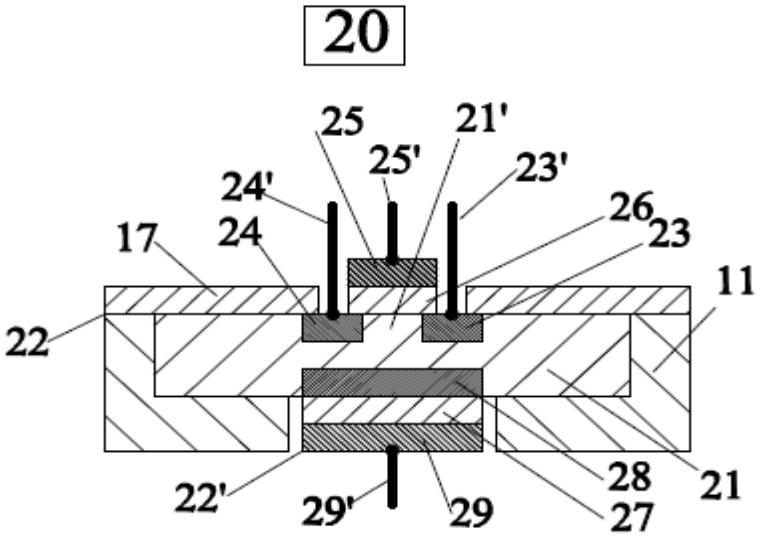


Figure 1B

Ingole Vijay Tulshiram
Ingole Indira Vijay
Ingole Ashutosh Vijay

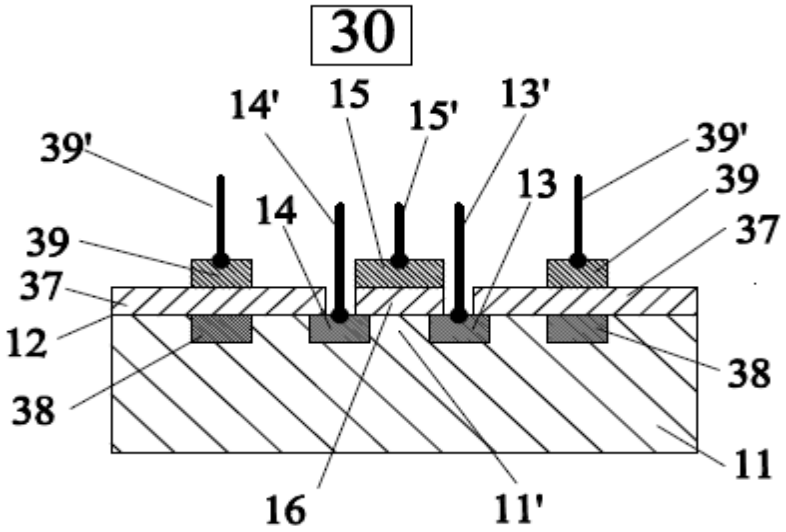


Figure 2A

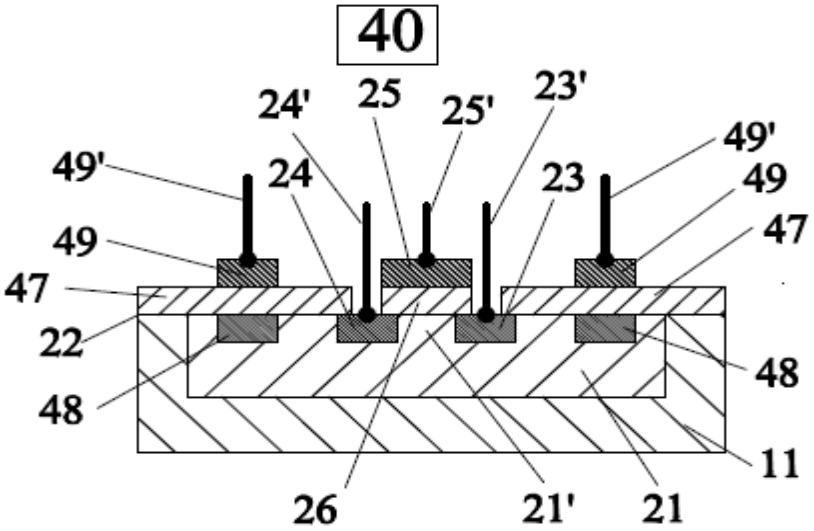


Figure 2B

Ingole Vijay Tulshiram
Ingole Indira Vijay

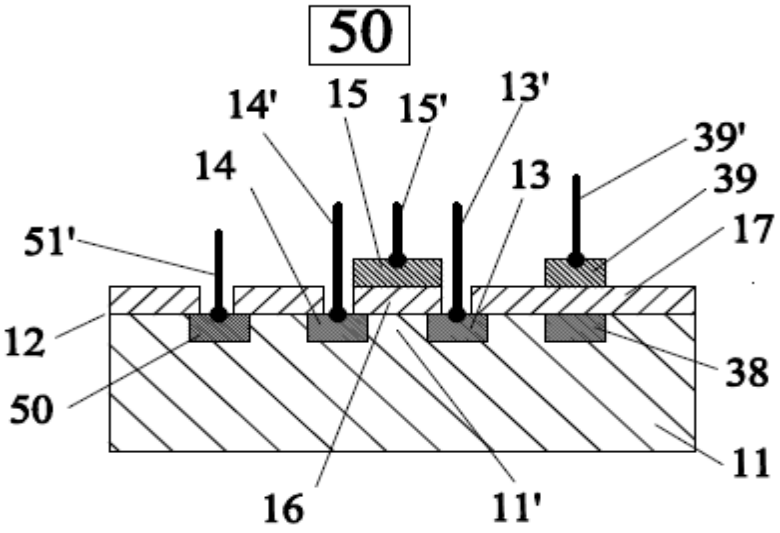


Figure 3A

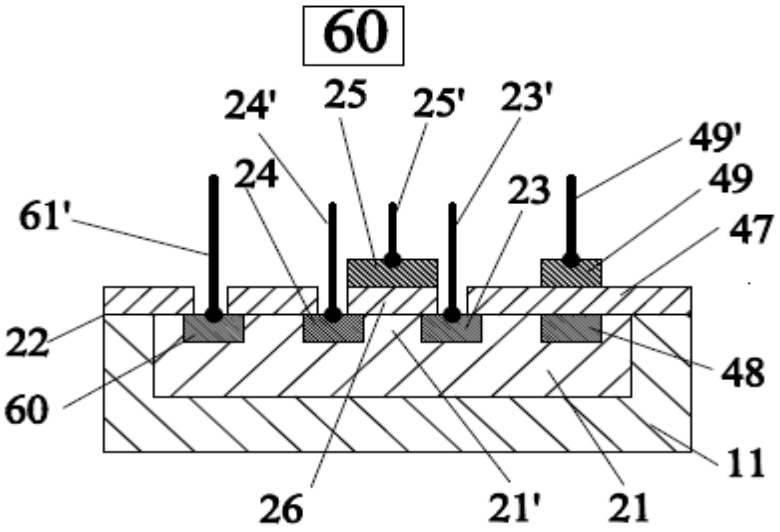


Figure 3B

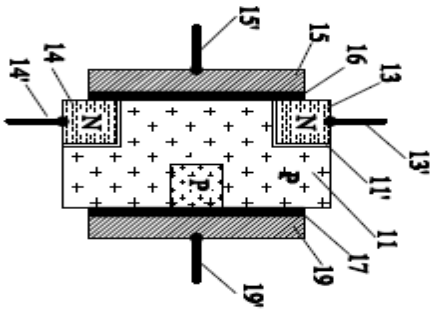


Figure 4A

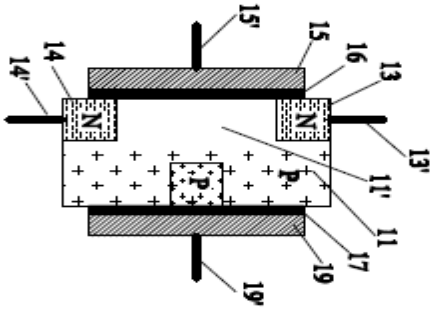


Figure 4B

70

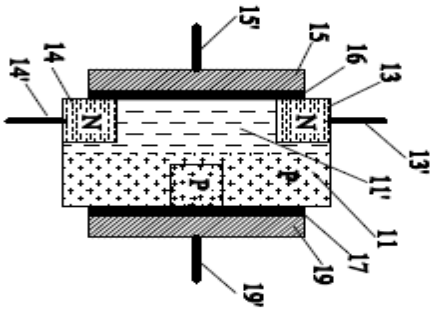


Figure 4C

Ingole Vijay Tulshiram
Ingole Indira Vijay
Ingole Ashutosh Vijay

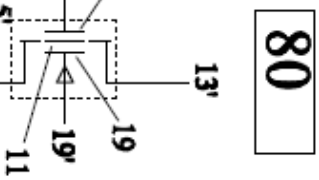


Figure 5A

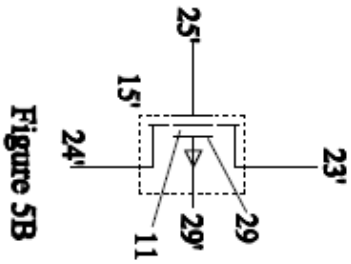


Figure 5B

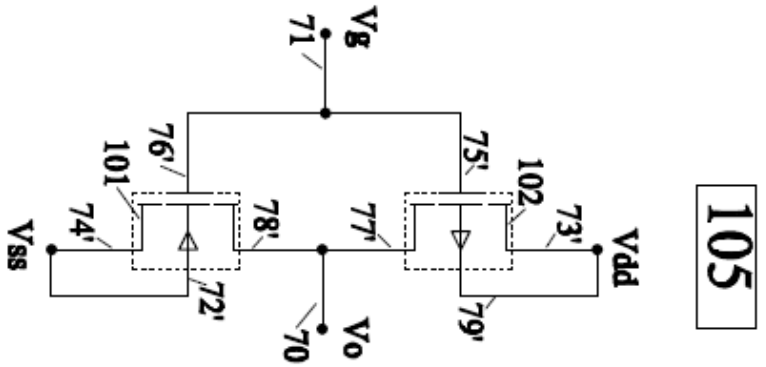


Figure 6A

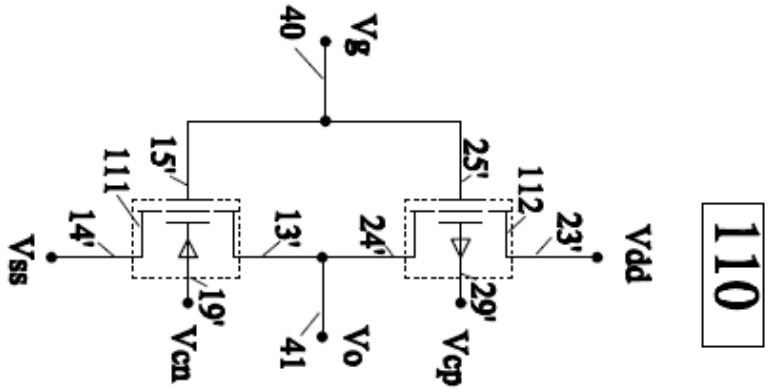


Figure 6B

Ingole Vijay Tulshiram
Ingole Indira Vijay
Ingole Ashutosh Vijay

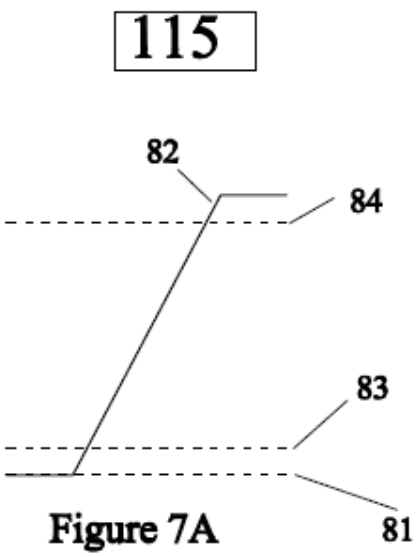


Figure 7A

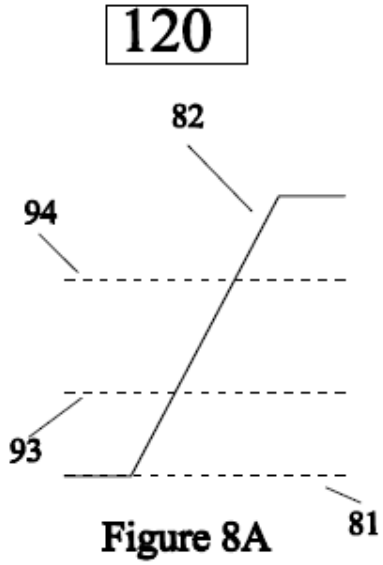


Figure 8A

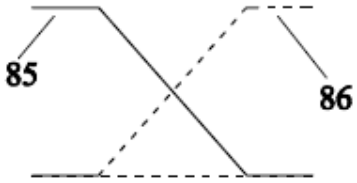


Figure 7B

Figure 8B

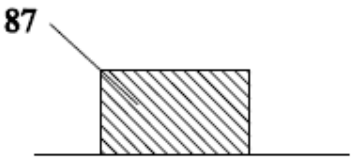


Figure 7C

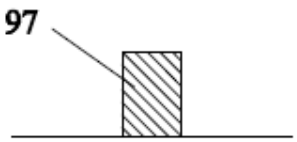


Figure 8C

Ingole Vijay Tulshiram
Ingole Indira Vijay
Ingole Ashutosh Vijay

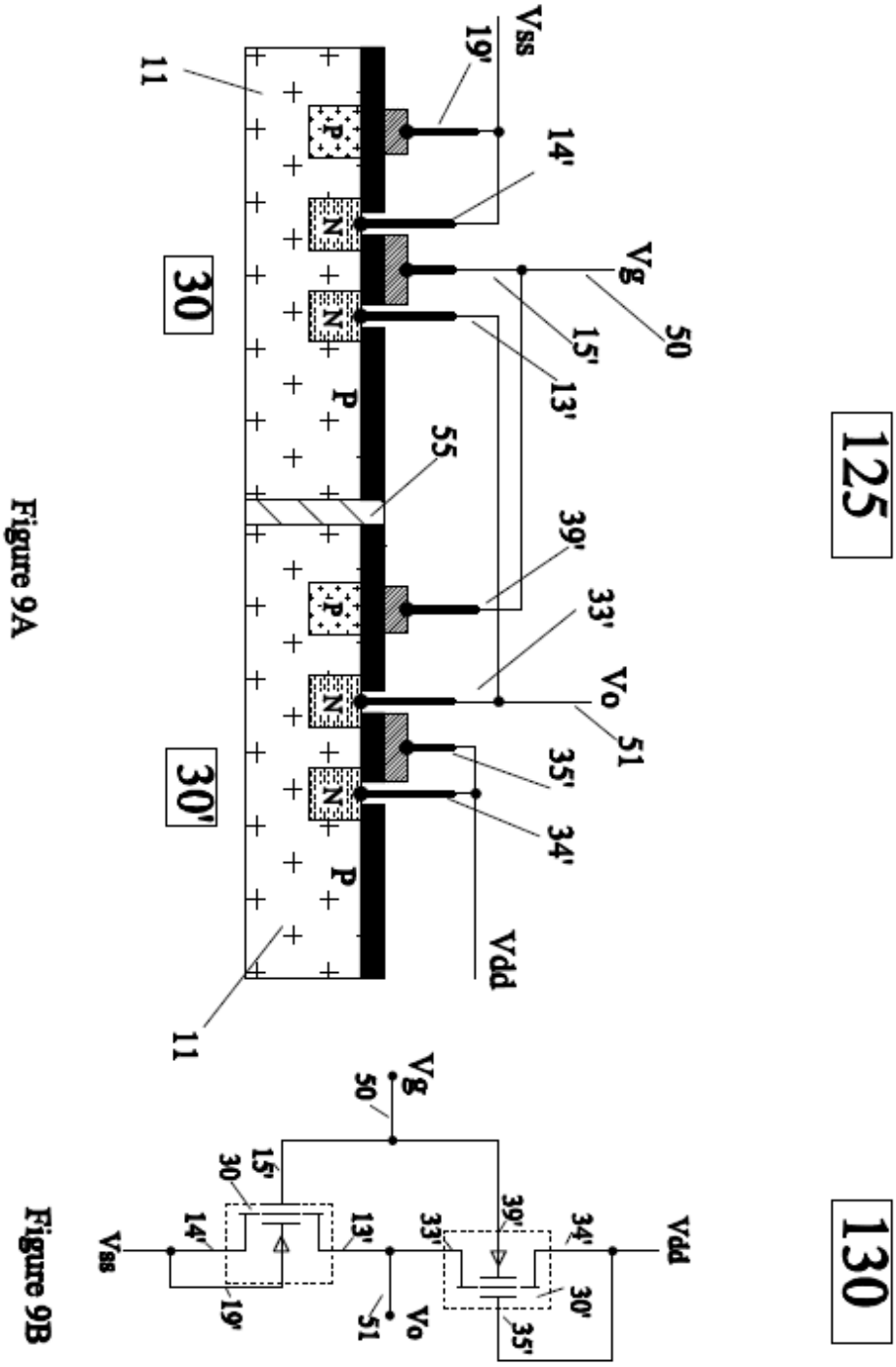
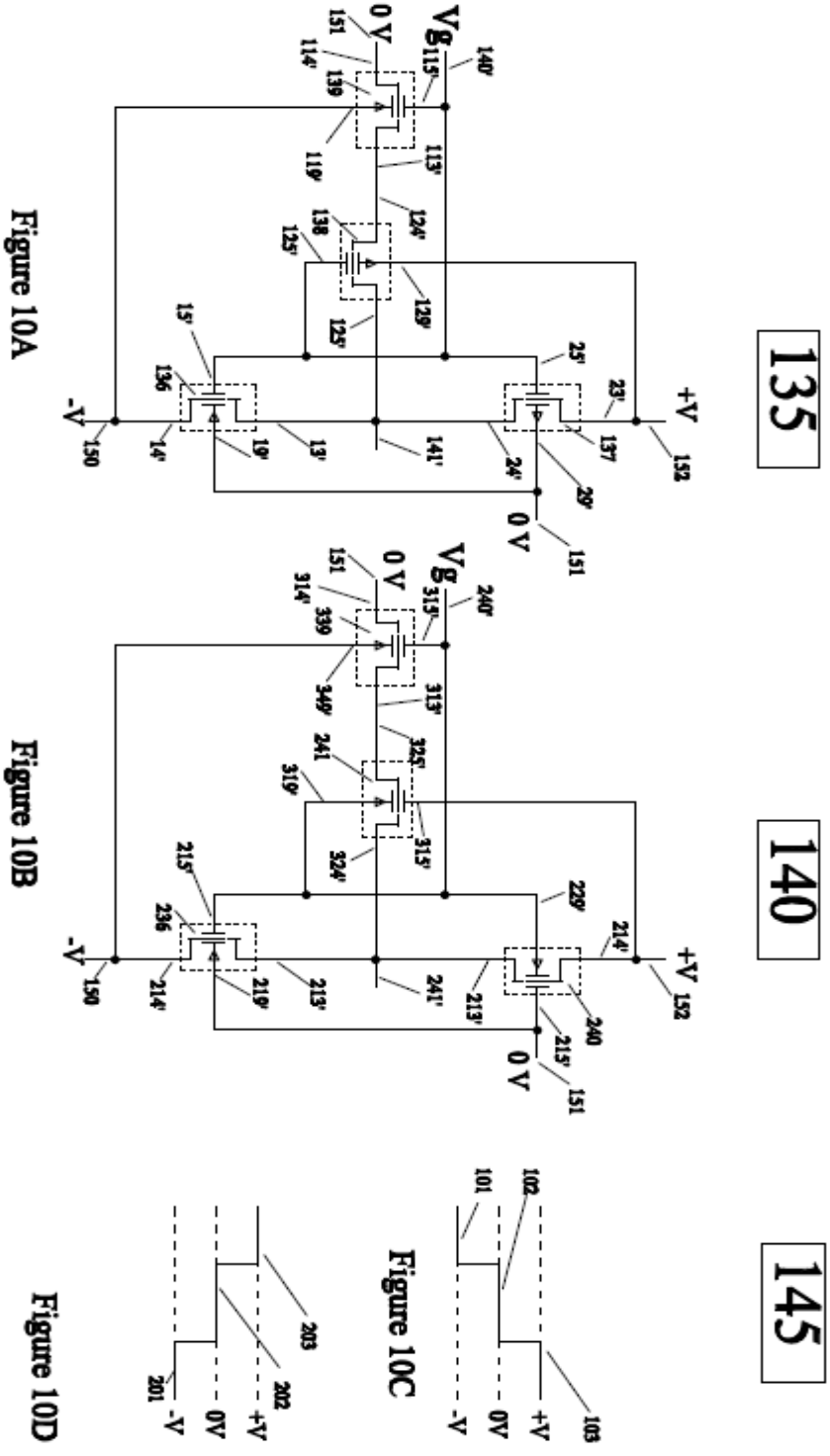


Figure 9A

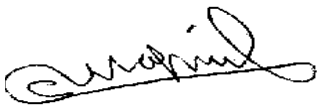
Figure 9B

Ingole Vijay Tulshiram
Ingole Indira Vijay
Ingole Ashutosh Vijay


135
140
145
Vg
0 V
+V
-V
0V
Figure 10A
Figure 10B
Figure 10C
Figure 10D

ABSTRACT

The objective of the present description of the said invention is to provide a VTI-MOSFET, may be an enhancement type, in N type and P type categories, and may be working solo or in tandem or singly or complimentary formation and each is having a drain, a source, a front gate means gate means first gate and proposed insulated back-gate means complimentary gate wherein the said MOSFET comprises a complimentary gate being disposed on the top of insulation layer being disposed on the semiconductor substrate layer and wherein the complimentary gate terminal comprises suitable conducting contact material, may be in the form of poly-silicon or any other suitable material for further electric connection; thus the said substrate is being insulated through a capacitive path thereby rendering freedom to the said complimentary gate connection to any voltage within the circuit topology without undue leakage, as against CMOS devices in the prior art and the device under disclosure operates due to difference of voltage between front gate and complimentary gate thereby N-MOSFET can replace P-MOSFET and vice the versa, and due to such unique characteristic, conventional CMOS topology in prior art be replaced by either N-type or P-type MOSFET devices means complimentary devices dispensed with, and preferably by N-type devices which renders high switching speed due higher mobility of charges and further a much economical, faster, simpler processing and fabrication and further switching characteristic of the said devices be controlled externally by suitably biasing the front gate or insulated back gate; and hitherto referred to as VTI-MOSFET.



Adv. Swapnil Gawande (IN/PA/1587)