FORM 1 (FOR OFFICE USE ONLY)

THE PATENT ACT 1970
(39 OF 1970) Application number:
And Filing date:
The patent rules, 2003 amount of fee paid:
CBR NO:

APPLICATION FOR GRANT OF PATENT
[See sec 7, 54,135 and rule20 (1)]

1 APPLICANT(S)

Name	Nationality	Address
Ingole Vijay Tulshiram	Indian	104 Ganediwal layout, camp, Amravati-444602
Ingole Ashutosh Vijay	Indian	104 Ganediwal layout, camp, Amravati-444602
Ingole Paritosh Vijay	Indian	104 Ganediwal layout, camp, Amravati-444602

2 Inventor(s)

Name	Nationality	Address
Ingole Vijay Tulshiram	Indian	104 Ganediwal layout, camp, Amravati-444602
Ingole Ashutosh Vijay	Indian	104 Ganediwal layout, camp, Amravati-444602
Ingole Paritosh Vijay	Indian	104 Ganediwal layout, camp, Amravati-444602

3. TITLE OF INVENTION
Flash analog to digital converter.

4. ADDRESS FOR CORRESPONDANCE OF APPLICANT IN INDIA:-
104 Ganediwal layout, Mobile number: 9422156677
Camp, E-mail:vijayingole@hotmail.com
Amravati-444602

5. DECLARATION:

(i) Declaration by the inventors

We the above named inventors are the true and first inventors for this invention
Date 21st day of November 2009

Signature of the inventors.

Name: (1) Ingole Vijay Tulshiram

(2) Ingole Ashutosh Vijay

(3) Ingole Paritosh Vijay

(ii) Declaration by the applicants

We the applicants hereby declare that:-
We are in possession of above mentioned invention.
The complete specification relating to the invention is filed with the application
There is no lawful ground of objection to the grant of patent to us.

6. FOLLOWING ARE THE ATTACHMENTS WITH THE APPLICATION

(a) Complete specification in duplicate

(b) Drawings in duplicate

(c) Statement and undertaking on form 3 in duplicate

(d) Abstract in duplicate

(e) Drawing in duplicate

(f) Power of authority.

(g) Form number 9.

(h) Form number 18.

Fee Rs in Cash/Cheque/bank draft bearing no

Date on Bank.

We hereby declare that to the best our knowledge, information and belief the facts and the matter stated herein are correct and we request that the patent may be granted to us for the said invention.

Dated this 21st day of November 2009

Signature:
Name :(1) Ingole Vijay Tulshiram
(2) Ingole Ashutosh Vijay
(3) Ingole Paritosh Vijay

FORM 2

THE PATENT ACT 1970
(39 OF 1970)
AND
The patent rules, 2003

COMPLETE SPECIFICATION
(See section 10: rule 13)

1. TITLE OF INVENTION

Flash analog to digital converter.

2 APPLICANTS(S)

Name	Nationality	Address
Ingole Vijay Tulshiram	Indian	104 Ganediwal layout, camp, Amravati-444602
Ingole Ashutosh Vijay	Indian	104 Ganediwal layout, camp, Amravati-444602
Ingole Paritosh Vijay	Indian	104 Ganediwal layout, camp, Amravati-444602

3. PREAMBLE TO THE DESCRIPTION

COMPLETE

Following specification particularly describes the invention and the manner in which it is to be performed.

DESCRIPTION:-

1. Field of the Invention:

This invention relates to an analog to digital converter (ADC) circuit and more particularly to flash analog to digital converter and still more specifically to higher bit low component count flash ADC circuits which can be fabricated in integrated circuit form.

2. USE OF INVENTION:

Following invention is useful for the purpose of optimizing flash ADC circuit which is simple, having low component count, low number of switches, low current requirement and where all bit circuits are similar to enhance resolution, which is predisposing factor to reduce layout area

requirement of integrated circuit fabrication technology, being a limiting factor in the present integrated circuit flash A/D converters.

2. Prior Art:

High speed integrated circuit A/D converters have been provided in the prior art for the purpose of rapid conversion of analog signals to digital form for digital processing. The state of the art in such flash A/D converters is summarized by Anvekar O.K. et al, Ed., "Electronic Data Conversion", Tata McGraw-Hill Publishing Company Ltd. (ISBN 0-07-462009-6).

As ADC forth in this prior art, conventional A/D converters with n-bit resolution require (2.sup.n - 1) comparators, or 255 comparators for an 8 bit resolution flash converter and 4092 comparators in the case of a 12 bit resolution flash converter. The necessity to provide such large numbers of comparators in these prior art flash conveners means that 8 bit resolution is the limit in currently available integrated circuit flash A/D converters, with 12 bit resolution converters being considered for future products with further improvements in integrated circuit fabrication technology..

PROBLEM TO BE SOLVED:

Quite a few improvements in flash A/D converter design have been reported having reduced number of comparators per bit output but they still suffers from the higher component count, complex semiconductor switches, large number of current buses, high current requirement and circuit complexity. Therefore, a need arises for an optimized flash ADC circuit which is simple, having low component count, low number of switches, low current requirement and where all bit circuits are similar to enhance resolution, which is predisposing factor to reduce layout area

requirement of integrated circuit fabrication technology, being a limiting factor in the present integrated circuit flash A/D converters.

OBJECT:

Accordingly, it is an object of this invention to provide an improved flash A/D convener circuit design in which integrated circuit fabrication technology is removed as a limiting factor in the resolution of the converter.

It is another object of the invention to provide a flash A/D converter in which the number of comparators in the converter does not increase exponentially with an increasing bit resolution of the converter.

It is a further objective of the invention to provide a flash A/D converter in which the total current requirement in the converter need not increase exponentially with an increasing bit resolution of the converter.

It is a still further objective of the invention to provide a flash A/D converter in which switches are voltage operated thereby eliminating the number of current buses and current operated switch complexity and the number thereof.

It is a further objective of the invention to provide a flash A/D converter in which digitized voltage output or quantized output (digital equivalent of the analog input) is directly available without the use of external digital to analog converter (DAC).

BEST MODE OF WORKING:-

The attainment of the foregoing and related objects may be achieved through use of the novel flash A/D converter herein disclosed. In accordance with this invention, an A/D converter provides a multiple bit, parallel output arranged in higher significant to lower significant bits and comprising means for providing an analog input voltage signal as a parallel input to each of a plurality of generally replicated parallel converter stages, each stage hereinafter referred to as bit cell, and each bit cell comprises a bit dependent reference voltage, hereinafter referred to as binary reference voltage (BRV) source, derived from a current divider source and a resistance, hereinafter referred to as reference resistance, means the adjacent lower significant bit has half the value of the said binary voltage whereas the adjacent higher significant bit cell has twice of the said binary voltage and further the said bit cell comprises a comparator means for comparison of two voltages and the said comparator output is connected to a single pole single throw switch, generally known as SPST switch, which is further connected in parallel to a resistance, hereinafter referred to as digitized resistance, whereas one terminal, hereinafter referred to as lower end, is connected to the terminal of digitized resistance of adjacent lower bit cell, except in lowest significant bit (LSB) cell, and remaining terminal of the said digitized resistance, hereinafter referred to as higher end, is connected to the digitized resistance of adjacent higher significant bit cell, except in most significant bit (MSB) cell where it is connected to ground and one of the input terminals of the said comparator is connected to the said lower end of the said digitized resistance whereas remaining input terminal of the said comparator of the said bit cell is connected to an analog input signal, means providing parallel analog input to all bit cells, hereinafter referred to as common analog input signal, and the said comparator compares the said input voltage with its other input terminal

voltage having the said common input signal voltage such that the voltage on the said higher end of the said digitized resistance is less than the said common input signal voltage the output of the said comparator goes to a logical T state and actuates the said SPST switch thereupon the said SPST switch, which is hitherto short circuiting the said digitized resistance, removes the short circuit across the said digitized resistance thereby higher end of the digitized resistance from the adjacent lower bit cell is connected to the lower end of digitized resistance of the adjacent higher bit cell through the said digitized resistance with associated BRV of the said bit cell and due to the typical circuit configuration the voltage (BRV) across the said reference resistance is equal to voltage across the said digitized resistance pertaining to the said bit cell under said condition of the said SPST switch and thus the net voltage available on the lower end, hereinafter referred to as voltage on bit cell, of digitized resistance of 'mlh cell means on the higher end of digitized resistance of (m+l)"1 cell, except MSB where it is connected to ground hence zero, is dependent on the logical state of the adjacent higher significant bit cells including MSB and such voltage on mth cell for 'n' stage ADC can be expressed in the form of an equation given by:

Where 'n'= number of bit cells/stages andn-l= next lower bit cell,

Vdm= voltage on ml bit cell = logical sum of the digital voltages (BRV) at the bit cell

including higher bit cells = quantized voltage

Vri = reference voltage of lowest significant bit cell

bm= logic state of mth bit cell iebm=l for logic T state andbm=0 for logic '0' state,

means logical state T will add and logical '0' will have no effect, of the plurality of

comparator output and on the contrary depending upon the inputs to the said comparator if its output does not change means logical state '0' then the output of the lower end of the digitized resistance of the adjacent more significant bit cell is directly connected to the higher end of the digitized resistance of the adjacent lower bit cell means bypassing the said bit cell BRV thereby logical state '0' of the said bit cell will not affect the binary voltage on the adjacent lower bit cell binary voltage and thus bit binary voltage is added in sequence from most significant bit to least significant bit in series depending upon the logical state of the individual bit cell and whereas the comparator of MSB receives its bit dependent binary voltage all the time and thus the said plurality of converter stages further being configured to carry out conversion of the analog input signal to a plurality of parallel digital output bits from said converter simultaneously in a flash manner and A further providing quantized output from the least significant bit cell, As a result, adding additional converter stages to the flash A/D converter of this invention increases circuit complexity only linearly, rather than exponentially, as in the case of prior art flash A/D converters. It is apparent from the aforesaid description that the total circuit current increases exponentially with the number of bit cells in a stage however, due to typical circuit configuration a stage comprising number of bit cells can be connected so as to form a pack. Though such a configuration reduces the circuit current requirement only linearly instead of exponentially but increases the number of current sources and drains however the optimum combination of number of bits per stage and total number of stages in a pack can be achieved by design trade off. In a pack the maximum number of stages comprising number of bit cells that can be convened in parallel is not limited by circuit, but by the accuracy in

manufacture of the current division, offset voltages and the speed of comparators and switches.

The attainment of the foregoing and related objects, advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention, taken together with the drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a circuit diagram of a flash ADC which illustrates a typical 4 bit ADC with provisions for expansion to V bit resolution in accordance with the invention.

FIG. 2 shows a circuit diagram of a typical bit cell of a flash flash ADC, which illustrates the expansion lines comprising FIG. 1 in accordance with the invention.

FIG. 3 shows a circuit diagram of ADC, which illustrates a typical 4 bit ADC with provisions for expansion to 'n' bit resolution without a provision for a quantized output in accordance with the invention having fewer components.

FIG. 4 shows a circuit diagram of ADC, which illustrates a typical 4 bit ADC with

provisions for expansion to 'n' bit resolution with a provision for a quantized and Vi LSB error and window comparator and control for output latch in accordance with the

invention.

FIG. 5 shows a circuit diagram of ADC, which illustrates an ADC with typical 2 stages of 2 bit cell each with provisions for expansion to 'n' bit resolution with reduced current drain and with a provision for a quantized output in accordance with the invention having fewer components.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings, more particularly to FIG. 1, there is shown a 4 bit flash A/D converter stage 10, with interconnection lines 102, 112, and 96 for expansion of the converter 10 to 'n' higher bit cells. The converter 10 includes four stages means bit cells 20,40,60, and 80. Each of the stages 80-20 has a divide-by-2 current source 180,160,140, and 120 respectively. '201 denotes the least significant hit (LSB). The most significant bit (not shown) of the comparator receives an input to its divide-by-2 current source (also not shown) on line 101 from a current source 100. The input to divide-by-2 current source 180 is supplied on line 102 by another divide-by-2 current source (not shown) of a next adjacent lower significant bit stage of the converter. An output from the divide-by-2 current source 180 is supplied on line 103 as an input to divide-by-2 current source 160. An output from divide-by-2 current source 160 is supplied on line 104 as an input to divide-by-2 current source 140. An output from divide-by-2 current source 140 is supplied on line 105 as an input to divide-by-2 current source 120. Because divide-by-2 current source 120 is part of the least significant bit 20, its output 106 is supplied on line 35 in to the same stage 20. The remaining outputs from divide-by-2 current sources 180,160,140, and 120 are also supplied to lines 81,61,41, and 21 respectively to line 82,62,42, and 22 of said reference resistances 89,69,49, and 29 and also to line 86,66,46, and 26 as input to comparators 91,71,51, and 21 of the stages 20,40,60, and 80 respectively. Line 83,63,43 and 23 of said reference resistance 89,69.49, and 29 and line 94,74,54,and 34 are connected to line 96,95,75, and 55 respectively. Line 98,78,58, and 38 of

said digitized resistance 93,73,53, and 33 and said SPST switch 92,72,52, and 32 line 84,64,44, and 24 of are connected to line 96,95,75, and 55 respectively. Line 97,77,57, and 37 of said digitized resistance 93,73,53, and 33 and said SPST switch 92,72,52, and 32 line 85,65,45 and 25 are connected to line 95.75,55, and 35 respectively. SPST switch 92,72,52, and 32 remaining line 84,64,44, and 24 and line 97,77,57, and 37 of digitized resistance 93,73,53, and 33 are connected to line 94,74,54, and 34 respectively. Output line 99, 79, 59, and 39 of the comparator 91, 71, 51, and 31 is connected to ADC digital output line 90, 70, 50, and 30 respectively. Output line 99, 79, 59, and 39 of the comparator 91, 71, 51, and 31 is connected to control line 88, 68, 48, and 28 of SPST switch 92, 72, 52, and 32 respectively. An analog signal to be converted to digital form by the ADC 10 is supplied online 110 as an input to buffer amplifier 109 (optional). The output 111 of buffer 109 is supplied to input line 87, 67, 47, and 27 of comparator 91, 71, 51 and 31 respectively. The line 96 of higher significant bit 80 is connected to ground 108 through next higher bit stages (not shown). The line 35 of the least significant bit cell 20 is connected to line 107 as quantized output of the analog input to be converter.

In operation of the flash A/D converter 10, the SPST switch 92,72.52, and 32 is controlled by its associated comparator 91,71,51, and 31 by output line 99,79,59, and 39 respectively such that the voltage on line 63,43,23 and 106 is dependent on the sum of the voltage of the adjacent higher bit cells, depending upon the state of the said SPST switches. Similarly the voltage on line 96 is the sum of the voltages across the SPST switches (not shown) of the adjacent higher bit cells (also not shown). Current flowing in line 35 means 34 is half of the total current of divide-by-2 current of source 120 of the least significant bit cell 20; current flowing in

line 55 is the sum of current of line 34 means line 35 and the reference current from reference current source 120 in line 22 means line 23; similarly current flowing in line 75 is the sum of current of line 54 means line 55 and the reference current from reference current source 140 in line 42 means line 43; similarly current flowing in line 95 is the sum of current of line 94 means line 95 and the reference current from reference current source 160 in line 62 means line 63; similarly current flowing in line 96 is the sum of current of line 94 means line 95 and the reference current from reference current source 180 in line 82 means line 83. Due to typical circuit configuration the current on line 95,75,55, and 35 is mirror image of current on line 82,62,42, and 22 respectively and said reference resistance 89,69,49, and 29 and said digitized resistance 93,73,53, and 33 being equal, their respective voltage drops are equal whenever the respective SPST switch is in open condition. Voltage on line 86,66,46, and 26 is a sum of voltage drop on reference resistance 89,79,59, and 39 and the voltage on line 96,95,75, and 55 respectively. The voltage on line 96,95,75, and 55 is the quantized voltage of the respective higher bit cells except MSB bit cell (not shown and which is at ground 108 voltage) to which bit dependent or quantized voltage of bit cells 80,60,40, and 20 is added. Such corrected quantized voltage is available on line 96,95,75,55, and 35 for the bit cell 80, 60, 40, and20 respectively. The corresponding bit dependent voltage (BRV) on line 82, 62, 42, and 22 is added to the respective quantized voltage of the next higher bit cells for the operation of operational amplifier 91, 61, 51, and 31 respectively as explained elsewhere. However the quantized voltage thus available on line 107 of LSB is taken out as final ADC quantized voltage output. The maximum number of bits that can be converted in parallel is not limited by circuit, but by the accuracy in manufacture of the current division, offset voltages and the speed of

comparators and switches. It should now be readily apparent to those skilled in the art that though only four bits are shown in the referred embodiment, the invention can be extended to any number of bits thereby increasing the resolution of the flash ADC described herein. A flash A/D converter capable of achieving the stated objects of the invention have been provided with only one line for cascading the multiplicity of bits. Because only one comparator needs be provided for each bit of resolution in the flash A/D converter described in this invention, the number of circuit elements required in the converter does not increase exponentially with each additional bit ot resolution added to the converter. Further the components of the set comprising bit cells, including the passive elements such as the reference resistances and the quantized resistances are of the same value thereby providing an extra advantage in fabrication. As a result, fabrication technology for an integrated circuit incorporating the flash A/D converter of this invention is not a limiting factor in the resolution of the converter. Still further it will be readily recognized by those skills in the art that for the circuit described herein the total current requirement of set increases exponentially with the number of bits. FIG. 2 shows a circuit diagram shows a typical bit cell 40 of a flash ADC, which illustrates the extension lines 104,112 and 75 for adjacent higher significant bit cell 60 and similarly extension lines 105,112 and 55 are for adjacent lower bit cell 20 comprising FIG. 1 in accordance with the invention.

FIG. 3 shows a circuit diagram of another preferred embodiment of ADC as described and illustrated in Fig. 1 but without a provision for a quantized output in accordance with the invention thus SPST switch 32, digitized resistance 33 and current divider 120 components comprising FIG. 1 are deleted.

FIG. 4 shows a circuit diagram of another preferred embodiment of ADC as described and illustrated in FIG. 1, but with higher resolution of 14 LSB and a latched digital output. To achieve the said higher resolution and to facilitate further desired interface, following components are added such as a buffer adder 109 with additional l/i LSB voltage input, a window comparator l19 which has inputs 126 and 112 and output 121 to control a logic gate 122, the logic gate 122 which has control inputs 120 (generally known as synchronizing signal) and 121 and output line 123 to control a latch 113 and the latch which has a control input 114 through 123 and digital inputs 90,70,50, and 30 corresponding to latched ADC output line 220, 240,260, and 280 respectively. FIG. 5 shows a circuit diagram of still another preferred embodiment of ADC as described and illustrated in FIG. l, wherein a pack comprising stage 12 having bit cells 20, 40 (though the stage may consists of number of bit cells but are not shown for the simplicity of illustration) and stage!3 with bit cells 60,80 is illustrated. The stage 12 is connected to next higher stage (not shown). The stage 12, 13 is connected to reference current source 100, 141 respectively and further connected to reference current drain 126, 125 respectively. Source 100 is a mirror image of source 26 and similarly sources 141 is a mirror image of source! 25. Line 57 of stage 13 is connected to line 75 of stage 12. Though such an arrangement requires more current sources and as well as current drains but generally reduces overall circuit current requirement. In a pack the maximum number of sets comprising number of bit cells that can be converted in parallel is not limited by circuit, but by the accuracy in manufacture of the current division, offset voltages and the speed of comparators and switches. It should now be readily apparent to those skilled in the art that though only two sets each comprising only two bits are described to in the present embodiment, the invention can be extended

to any number of bits and any number of sets thereby increasing the resolution of the flash ADC described herein thereby providing an extra advantage in fabrication. Still further it will be readily recognized by those skill in the art that the circuit described herein that a quantized output is readily available for further control without the need of additional digital to analog converter (DAC). Still further it will be readily recognized by those skill in the art that the circuit described herein that though the total current requirement of a set increases exponentially with the number of bits, the total current requirement of the pack comprising number of sets increases only linearly with number of sets therein. A flash A/D converter capable of achieving the stated objects of the invention has been provided. It will be readily recognized by those skill in the art further that though the components of the set comprising bit cells, including the passive elements such as the reference resistances and the quantized resistances are of the same value for the circuit configuration so far described in each set, circuit can work with a unique combination of different reference current, reference resistance and digitized resistance and further if same current in each set is desired, the values of the reference resistances and the quantized resistances are bit dependent means they increase exponentially with the higher significant set. Still further it will be readily recognized by those skill in the art that the circuit described herein that though the total current requirement of a set increases exponentially with the number of bits, the total current requirement of the pack comprising number of sets increases only linearly with number of sets in each pack. As a result, fabrication technology for an integrated circuit incorporating the flash A/D converter of this invention is not a limiting factor in the resolution of the converter. It should further be apparent to those skilled in the art that various changes in form and details of the invention as shown and described in Fig. 3 may be

made. For example, the bit outputs may be connected to latch to get a synchronized output through a synchronizing clock. A window comparator may be connected between analog input line and quantized output line to indicate completion of analog to digital conversion to be used for further control and further if a quantizing error of '/2 LSB is required then certain modification in the buffer amplifier 109 may have to be made i.e.LSB equivalent voltage may be added to the analog input. It should further be apparent to those skilled in the art that various changes in form and details of the invention as shown and described in Fig. 4 may be made. For example, if quantized output is not desired then in LSB 20 switch 32, current divider 120 and digitized resistance 33 may not be required however, certain change in the value of reference resistance 29 may be needed. It should further be apparent to those skilled in the art that various changes in form, combination thereof and details of the invention as shown and described may be made to suit particular requirement or requirements.

Claims :-

We Claim:

1. In accordance with this invention, an A/D converter provides a set comprising multiple bit, parallel output arranged in higher significant bit cell to lower significant bit cell or stage and comprising means for providing an analog input voltage signal as a parallel input to each of a plurality of generally replicated parallel converter stages, each stage hereinafter referred to as bit cell, and each bit cell comprises a bit dependent reference voltage, hereinafter referred to as binary reference voltage (BRV) source, derived from a current divider source and a resistance, hereinafter referred to as reference resistance, means the adjacent lower significant bit has half the value of the said binary voltage whereas the adjacent higher significant bit cell has twice of the said binary voltage and further the said bit cell comprises a comparator means for comparison of two voltages and the said comparator output is connected to a single pole single throw switch, generally known as SPST switch, which is further connected in parallel to a resistance, hereinafter referred to as digitized resistance, whereas one terminal, hereinafter referred to as lower end, is connected to the terminal of digitized resistance of adjacent lower bit cell, except in lowest significant bit (LSB) cell, and remaining terminal of the said digitized resistance, hereinafter referred to as higher end, is connected to the digitized resistance of adjacent higher significant bit cell, except in most significant bit (MSB) cell where it is connected to ADC ground and one of the input terminals of the said comparator is connected to the said lower end of the said digitized resistance whereas remaining input terminal

of the said comparator of the said bit cell is connected to an analog input signal, means providing parallel analog input to all bit cells, hereinafter referred to as common analog input signal, and the said comparator compares the said input voltage with its other input terminal voltage dependent on the adjacent higher bit cell available on said higher end of the said digitized resistance hereinafter referred to as digitized • voltage, and if the said digitized voltage is less than the said common input signal voltage the output of the said comparator provides a logical T state of the said ADC and opens the said SPST switch, which is hitherto short circuiting the said digitized resistance, thereby to higher end of the digitized resistance from the adjacent lower bit cell a BRV of the said bit cell is added to the digitized voltage at the lower end of digitized resistance of the adjacent higher bit cell, else the comparator provides a logical '0' state of the said ADC and thence SPST switch remains closed and there no change of voltage due to the said bit cell on the adjacent lower bit cell and due to the typical circuit configuration the voltage (BRV) across the said reference resistance is equal to the voltage across the said digitized resistance pertaining to the said bit cell under open condition of the said SPST switch and thus to the net voltage available on the lower end , hereinafter referred to as voltage on bit cell, of the bit cell a respective BR.V is added in sequence from most significant bit to least significant bit in series depending upon the logical state of the individual higher bit cells and whereas the comparator of MSB receives its bit dependent binary voltage all the time and thus the said plurality of converter stages further being configured to carry out conversion of the analog input signal to a plurality of parallel digital output bits from said converter

simultaneously in a flash manner and further providing quantized output from the least significant bit cell and as a result, adding additional converter stages to the flash A/D converter of this invention increases circuit complexity only linearly, rather than exponentially, as in the case of prior art flash A/D converters.

2. The analog to digital converter of claim 1 in which each of the comparators comprises a differential amplifier.
3. The analog to digital converter of claim 1 in which each of the switches comprises a single pole single throw generally a semiconductor voltage operated switch.
4. The analog to digital convener of claim 1 in which each of said bit cell circuit is replicated to form a plurality of parallel converter stages thus forming a set.
5. The analog to digital converter of claim 1 in which each of said bit cell circuit is configured to provide its analog to digitally converted bit output.
6. The analog to digital converter of claim 1 in which each of said bit cell circuit is configured to provide its bit dependent reference voltage derived from a bit dependent current source and a reference resistance.
7. The analog to digital converter of claim 1 and 4 in which each of the said reference resistance and the said digitized resistance are generally equal in magnitude means value.
8. The analog to digital converter of claim 1 and 7 in which each lower significant bit cell stage of said analog to digital converter includes a divide-by-2 current circuit which receives a current as an input from the current divider of the adjacent higher significant bit cell stage output, except in most significant bit cell stage receiving the current

reference signal as its input, and further the current divider of each stage providing its remaining divide-by-2 output as a current reference source supplying to the to the adjacent lower significant bit cell stage except in LSB.

9. The analog to digital converter claimed in preceding claims, comprising bit cells wherein the said comparator compares the said input voltage with its other input terminal voltage dependent on the adjacent higher bit cell available on said higher end of the said digitized resistance hereinafter referred to as digitized voltage, and if the said digitized voltage is less than the said common input signal voltage the output of the said comparator provides a logical T state of the said ADC and opens the said SPST switch, which is hitherto short circuiting the said digitized resistance, thereby to higher end of the digitized resistance from the adjacent lower bit cell a BRV of the said bit cell is added to the digitized voltage at the lower end of digitized resistance of the adjacent higher bit cell, else the comparator provides a logical '0' state of the said ADC and thence SPST switch remains closed and there no change of voltage due to the said bit cell on the adjacent lower bit cell and due to the typical circuit configuration the voltage (BRV) across the said reference resistance is equal to the voltage across the said digitized resistance pertaining to the said bit cell under open condition of the said SPST switch and thus to the net voltage available on the lower end , hereinafter referred to as voltage on bit cell, of the bit cell a respective BRV is added in sequence from most significant bit to least significant bit in series depending upon the logical state of the individual higher bit cells.

10. The analog to digital converter of claim Ho 9, wherein in each bit cell the said bit dependent current from said current divider source flows through the said reference resistance and the cumulative current from the adjacent lower significant bit cells flows through the said digitized resistance, whenever the said SPST switch is open under logical T state, and the said currents being the mirror image of each other therefore the voltages developed across each of the said resistances are same for the said bit cell.
11. The analog to digital converter of claim land 10 in which each of the said set comprising plurality of bit cell stages, the said bit reference currents arc bit dependent means increases exponentially means doubles for each adjacent higher bit means from least significant bit to most significant bit of the said set.
12. The analog to digital converter of claim 1 to 11 in which each of the said pack comprising plurality of sets and each set of the said sets comprising plurality of bit cell stages, wherein the least significant bit of the higher significant set is connected to most significant bit of the adjacent lower significant cell and at the junction of such sets and the ground a current drain, which is a mirror image of the said reference current source, is generally connected means the total current received from the reference current source means the next higher significant set current configuration remains unaffected.
13. The analog to digital converter of claim 1 to 12 in which each of the said pack comprising plurality of sets and each set of the said sets comprising plurality of bit cell stages, means each set is configured such that the current requirement of each set of the said pack is generally replicated thereby the total current requirement of the pack

is the sum of current sources of each set. means increases in arithmetic progression.

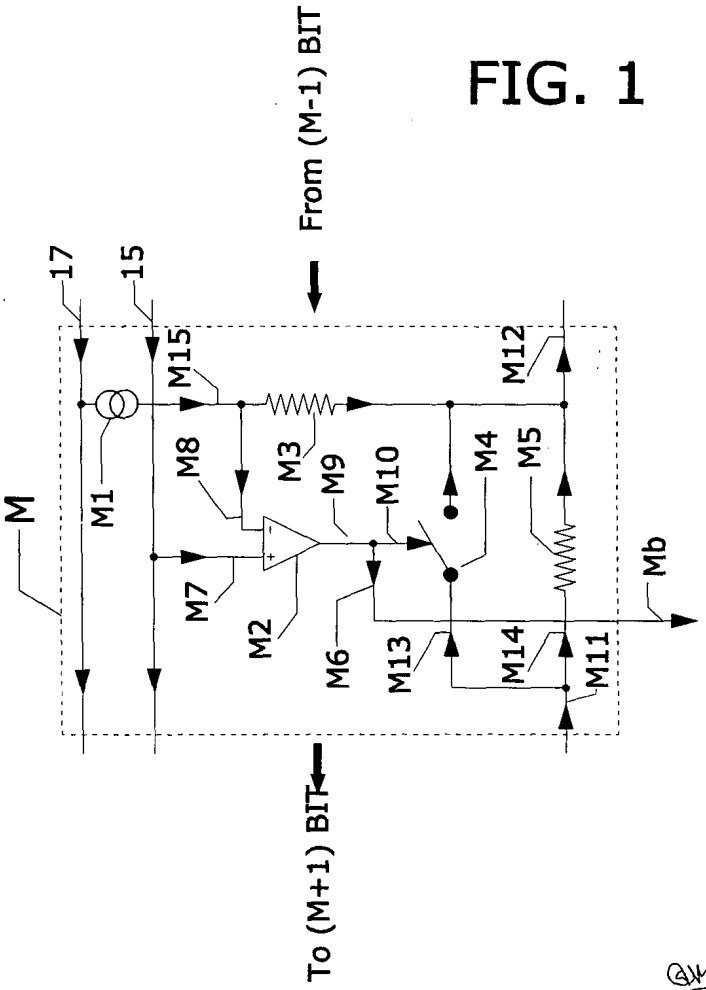
14. An analog to digital converter as in claims 1 to 13 comprising plurality of packs for providing a multiple bit, parallel output arranged in higher significant to lower significant bits comprising a plurality of parallel bit cell stages, in which each of the bit cell stages circuit configuration is generally identical in circuit component count and values thereof means circuit configuration of each bit cell stages is replicated to form plurality of multiple bit cell stages.
15. An analog to digital converter as in claim 1 and as recited in claim 2 to 14 and as described and illustrated in preferred embodiments and ascertain the nature of this invention and the manner in which it is to be performed and revealed in diagrams of FIG. 1, FIG. 2, FIG.3, FIG4, and FIG. 5.

*****

ABSTRACT:-

An analog to digital flash converter (ADC) is disclosed having a multiple bit, parallel digital output arranged in least significant (LSB) to most significant bits (MSB) each comprising a replicated individual stage of bit cell circuit configuration. The resolution of the said ADC depends upon the number of such bit cells. Each replicated bit circuit comprises a single bit having its bit dependent binary weighted voltage current , a single pole single throw analog switch, one comparator, two equal resistances, and one current divider source. The input analog voltage is connected to a plurality of the said arranged converter stages. The respective comparator in each bit cell compares the input analog voltage with its own binary weighted voltage available on its resistance added to the bit dependent binary weighted voltage depending upon the respective bit status, known as quantized voltage, of adjacent more significant bit cell. Whereas such voltage is independent of the analog signal input voltage but dependent on the binary state of the adjacent more significant bit cells quantized voltage available on their respective resistances and supplies to any adjacent lower significant bit cell. Comparators provide parallel digital bit out puts depending upon their respective binary status. The converter converts the analog input signal to digital output bits simultaneously in flash manner. The invention is further revealed in figure1 which shows circuit diagram of flash ADC with provision for expansion to ‘n’ bit resolution in accordance with the invention and further explained by figure2, figure 3, figure 4 and figure 5.

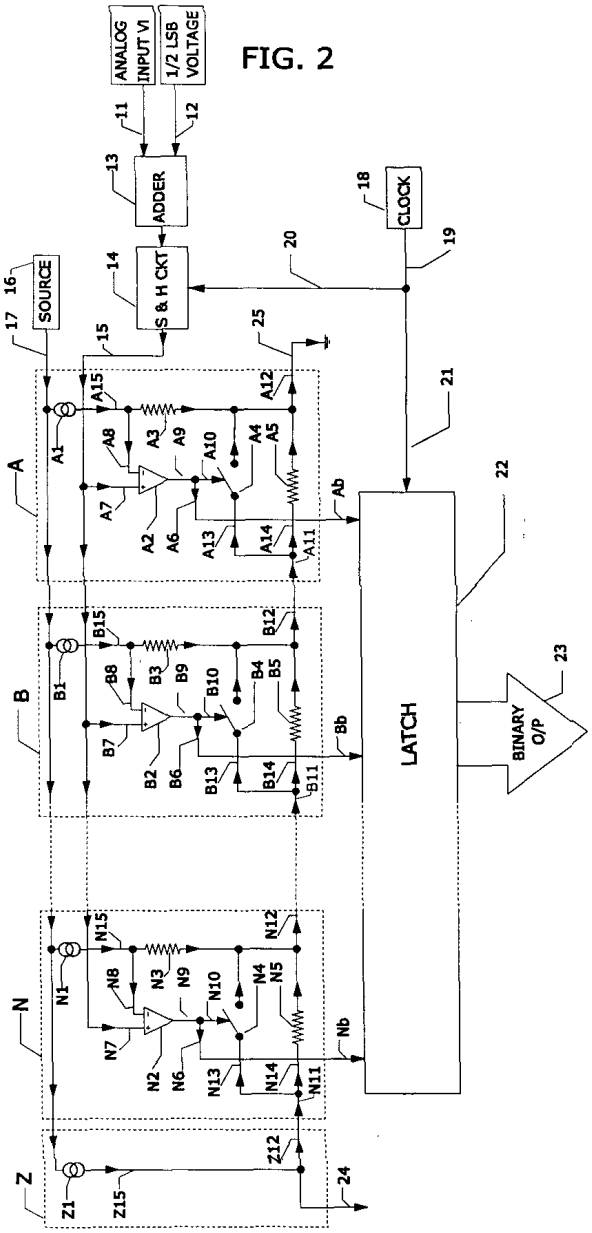
FIG. 1



Angole - Vijay Tulshiram.

Sheet 2/4.

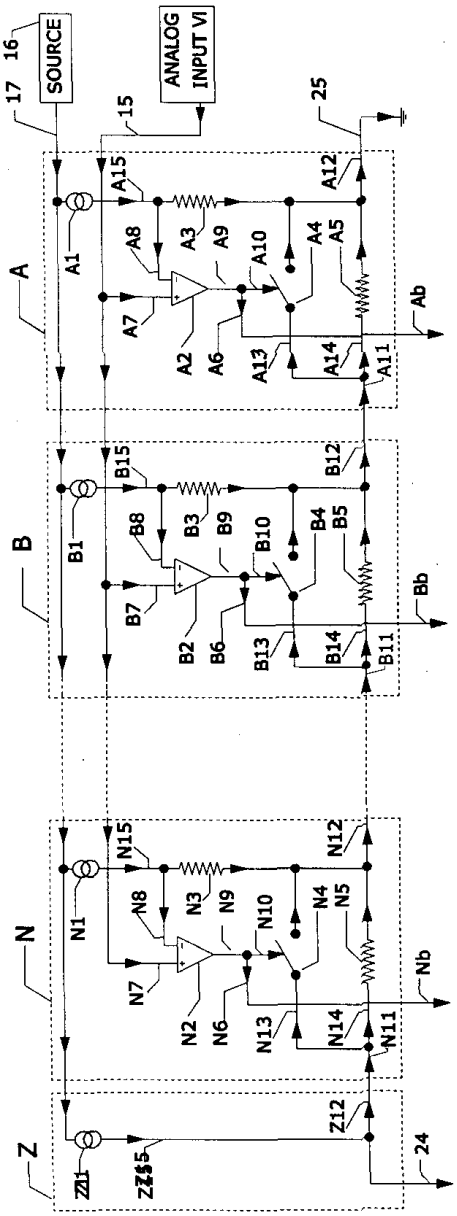
FIG. 2



Inventor Vijay Tulshibagwale

Sheet 3/4.

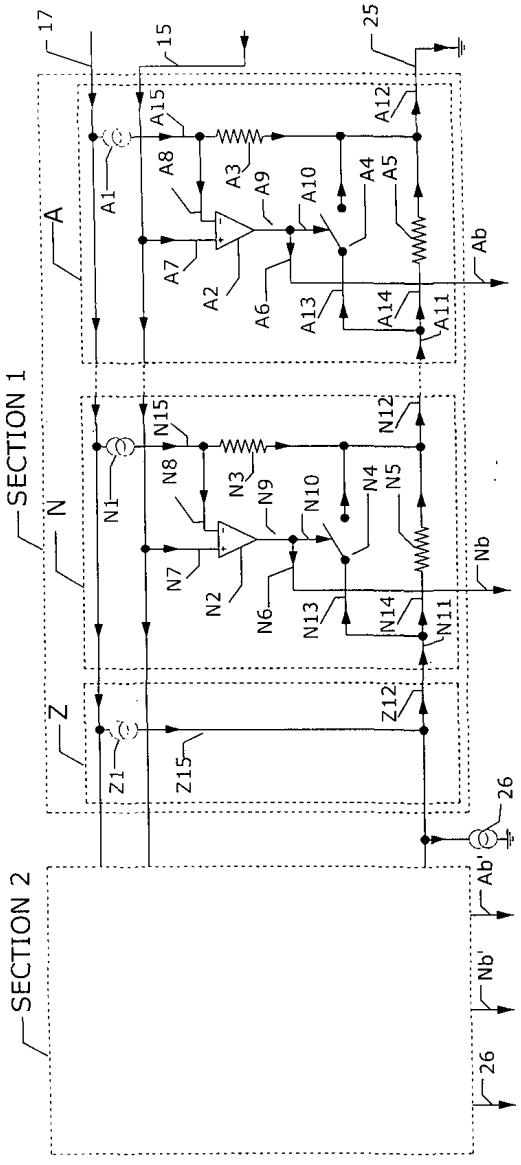
FIG. 3



21 DEC 2009

Impale Vijay Tuldhirm. Sheet 3/6.

FIG. 4



21 DEC 2009

FORM 3

THE PATENT ACT 1970
(39 OF 1970)
AND
The patent rules, 2003
STATEMENT AND UNDERTAKING UNDER SECTION 8
(See section 8; rule 12)

We

Name	Nationality	Address
Ingole Vijay Tulshiram	Indian	104 Ganediwal layout, camp, Amravati-444602
Ingole Ashutosh Vijay	Indian	104 Ganediwal layout,camp,Amravati-444602
Ingole Paritosh Vijay	Indian	104 Ganediwal layout,camp,Amravati-444602

Hereby declare:-
(i) that we have not made any this application for the same /substantially the same invention outside India.

Dated this 21st day of November 2009

Signature

To
The controller of patents,
The patent office,
At Mumbai.

FORM 9

THE PATENT ACT 1970
(39 OF 1970)

AND
The patent rules, 2003

REQUEST FOR PUBLICATION
(See section 11-A(2);rule24-A)

We

Name	Nationality	Address
Ingole Vijay Tulshiram	Indian	104 Ganediwal layout,camp,Amravati-444602
Ingole Ashutosh Vijay	Indian	104 Ganediwal layout,camp,Amravati-444602
Ingole Paritosh Vijay	Indian	104 Ganediwal layout,camp,Amravati-444602

Hereby request for early publication of our application no
Dated under section 11(a) 2 of the act.

Dated this 21st day of November 2009

Signature

To
The controller of patents,
The patent office,
At Mumbai.

FORM 18
THE PATENT ACT 1970
(39 OF 1970)
And

(FOR OFFICE USE ONLY)

Application number:
filing date:

The patent rules, 2003 amount of fee paid:

CBR NO:

REQUEST FOR EXAMINATION OF APPLICATION OF PATENT

[See section 11-B and rules 20(4)(ii),24-B(1)(i)]

1. APPLICANT

Name	Nationality	Address
Ingole Vijay Tulshiram	Indian	104 Ganediwal layout,camp,Amravati-444602
Ingole Ashutosh Vijay	Indian	104 Ganediwal layout,camp,Amravati-444602
Ingole Paritosh Vijay	Indian	104 Ganediwal layout,camp,Amravati-444602

We hereby request that our application for patent no
filed on Shall be examined under section 12 and 13 of the act.
Address for service: - 104 Ganediwal layout, camp, Amravati-444602.

Dated this 21st day of November 2009

Signature

To
The controller of patents,
The patent office,
At Mumbai