FORM 1 (FOR OFFICE USE ONLY)

THE PATENT ACT 1970
(39 OF 1970) Application number:
And Filing date:
The patent rules, 2003 amount of fee paid:
CBR NO:

APPLICATION FOR GRANT OF PATENT
[See sec 7, 54,135 and rule20 (1)]

1 APPLICANT(S)

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Ingole Ashutosh Vijay	Indian	104 Ganediwal layout, camp, Amravati-444602
Ingole Paritosh Vijay	Indian	104 Ganediwal layout, camp, Amravati-444602

2 Inventor(s)

Name	Nationality	Address
Ingole Vijay Tulshiram	Indian	104 Ganediwal layout, camp, Amravati-444602
Ingole Ashutosh Vijay	Indian	104 Ganediwal layout, camp, Amravati-444602
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3. TITLE OF INVENTION
Capacitor ladder flash analog to digital converter

4. ADDRESS FOR CORRESPONDANCE OF APPLICANT IN INDIA:-
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5. DECLARATION:

(i) Declaration by the inventors

We the above named inventors are the true and first inventors for this invention
Date 21st day of November 2009

Signature of the inventors.

Name: (1) Ingole Vijay Tulshiram

(2) Ingole Ashutosh Vijay

(3) Ingole Paritosh Vijay

(ii) Declaration by the applicants

We the applicants hereby declare that:-
We are in possession of above mentioned invention.
The complete specification relating to the invention is filed with the application
There is no lawful ground of objection to the grant of patent to us.

6. FOLLOWING ARE THE ATTACHMENTS WITH THE APPLICATION

(a) Complete specification in duplicate

(b) Drawings in duplicate

(c) Statement and undertaking on form 3 in duplicate

(d) Abstract in duplicate

(e) Drawing in duplicate

(f) Power of authority.

(g) Form number 9.

(h) Form number 18.

Fee Rs in Cash/Cheque/bank draft bearing no

Date on Bank.

We hereby declare that to the best our knowledge, information and belief the facts and the matter stated herein are correct and we request that the patent may be granted to us for the said invention.

Dated this 21st day of November 2009

Signature:
Name :(1) Ingole Vijay Tulshiram
(2) Ingole Ashutosh Vijay
(3) Ingole Paritosh Vijay

FORM 2

THE PATENT ACT 1970
(39 OF 1970)
AND
The patent rules, 2003

COMPLETE SPECIFICATION
(See section 10: rule 13)

1. TITLE OF INVENTION

Capacitor ladder flash analog to digital converter.

2 APPLICANTS(S)

Name	Nationality	Address
Ingole Vijay Tulshiram	Indian	104 Ganediwal layout, camp, Amravati-444602
Ingole Ashutosh Vijay	Indian	104 Ganediwal layout, camp, Amravati-444602
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3. PREAMBLE TO THE DESCRIPTION

COMPLETE

Following specification particularly describes the invention and the manner in which it is to be performed.

DESCRIPTION:-

1. Field of the Invention:

This invention relates to an analog to digital converter (ADC) circuit and more particularly to flash analog to digital converter and still more specifically to higher bit low component count capacitor ladder flash ADC circuits which can be fabricated in integrated circuit form.

2. USE OF INVENTION:

Following invention is useful for the purpose of converting analog electric signal in to digital signal by optimizing flash ADC circuit components which is fast, simple, having low component count, low number of comparators, and where all bit circuits are similar to simplify design, enhance resolution, which are predisposing factors to simplify design, reduce layout area requirement of integrated circuit fabrication technology, being a limiting factor in the present integrated circuit flash ADCs.

Prior Art:

High speed integrated circuit ADC have been provided in the prior art for the purpose of rapid conversion of analog signals in to digital form for digital processing. The state of the art in such flash ADC is summarized by Anvekar D.K. et al, Ed., "Electronic Data Conversion", Tata McGraw-Hill Publishing Company Ltd. (ISBN 0-07-462009-6).

As flash ADC in this prior art, conventional ADC with n-bit resolution require $(2^n - 1)$ comparators, i.e. 255 comparators for an 8 bit resolution flash converter, and 4092 comparators in the case of a 12 bit resolution flash converter. The necessity to provide such large numbers of comparators in these prior art flash converters means that 8 bit resolution being the limit in currently available integrated circuit flash ADCs, with 12

bit resolution converters being considered for future products with further improvements in integrated circuit fabrication technology. Quite a few improvements in flash ADC design have been reported having reduced number of comparators per bit output but they still suffers from the much higher component count, complex semiconductor switches, large number of current buses, high current requirement and circuit complexity. Therefore, a need arises for an optimized flash ADC circuit which is simple, having low comparator count, low power consumption and where all bit circuits are similar to facilitate design and fabrication, which is predisposing factor to reduce layout area requirement of integrated circuit fabrication technology, and being a limiting factor in the present integrated circuit flash ADC.

PROBLEM TO BE SOLVED:

Quite a few improvements in flash ADC design have been reported having reduced number of comparators per bit output but they still suffers from much higher component count, complex semiconductor switches, large number of current buses, high current requirement and circuit complexity. Therefore, a need arises for an optimized flash ADC circuit which is simple, having low comparator count, low power consumption, and where all bit circuits are similar to simplify design, enhance resolution, which is predisposing factor to reduce layout area requirement of integrated circuit fabrication technology, being a limiting factor in the present integrated circuit flash ADCs.

OBJECT:

Accordingly, it is an object of this invention to provide an improved flash ADC circuit design by which integrated circuit fabrication technology is no more a limiting factor in the resolution of the converter.

It is another object of the invention to provide a flash ADC in which the number of comparators in the converter are equal to the number of bits and does not increase exponentially..

It is a further objective of the invention to provide a flash ADC in which the sensing capacitors increases linearly with number of bits and the total power requirement in the converter is reasonably low even for higher resolution.

It is a further objective of the invention to provide a flash ADC in which the semiconductor switches requirement increases linearly with number of bits. In an ADC of previous art a 16 bit flash ADC requires 65,535 comparators and not mention about other circuit components where as the ADC of present invention requires only 16 comparators.

It is a further objective of the invention to provide a simple bit cell circuit which can be replicated and connected in series to enhance the resolution of ADC.

It is a further objective of the invention to provide a flash ADC in which parallel digital outputs are directly available without the use of complex encoder.

It is a still further objective of the invention to provide a flash ADC in which switches are voltage operated thereby eliminating the number of current buses and current operated switch complexity and the number thereof.

It is a further objective of the invention to provide a flash ADC in which digitized voltage output or quantized output (digital equivalent of the

analog input) is normally available without the use of external digital to analog converter (DAC).

BEST MODE OF WORKING:-

The attainment of the foregoing and related objects is achieved through use of the novel capacitor ladder flash ADC herein disclosed and according to this invention the analog to digital converter (ADC) for converting analog input signal into coded binary digital outputs comprising number of bit cells and each bit cell comprising of;

a reference voltage source;

a capacitor means coupled between next lower bit circuit and next higher bit circuit for providing binary reference voltage (BRV) ;

a first semiconductor switch means coupled between one end of capacitor and next lower bit circuit means connecting the capacitor across the respective reference voltage source and ground for providing reference quantitized voltage of the bit cell when first switch is deactivated means 'off' condition and second switch it is closed means 'on' condition;

a comparator means for comparing the input analog signal connected to non-inverting input and quantitized voltage of the bit cell connected to inverting input and controlling the first semiconductor switch means when the analog signal is greater than the quantitized voltage to close the semiconductor switch under digital '1' condition means activated otherwise open the semiconductor switch under digital '0' condition thereby connecting the quantitized voltage of next lower bit section to next higher bit circuit thereby bypassing the capacitor and to further means provide a digital out put of the ADC pertaining to that bit cell;

a voltage reference source means providing voltage proportional to the binary reference voltage (BRV) of the bit cell means voltage drop across the reference resistance;

a third switch means common to all the bit cells of ADC operated by

clock circuit means under activated condition by the clock circuit means closed condition connects the common bus of analog voltage to ground and isolated the input analog voltage from the common analog voltage bus of all bit cells; whereas when it is deactivated it connects the input analog signal to the common bus of analog voltage to all bit cells for ADC operation;

the voltage to the comparator inverting input means the quantitized voltage of the lower bit cells added to the BRV means the reference voltage acroos the capacitor due to the voltage of voltage source of the same bit cell;

the quantitized voltage of the bit cell under closed switch means under digital '1' condition means the binary dependent voltage means the voltage across capacitor and voltage due to the lower significant bits means quantitized voltage of lower significant bet cells is added means BRV added means to the quantitized voltage to the higher bit cells available on the other end of capacitor means to the higher bit cell and means its one terminal connected to the next lower bit cell with added BRV;

the quantitized voltage of the bit cell under deactivated switch condition means under digital '0' condition means the voltage across capacitor is by passed means not added to quantitized voltage of lower bit means directly available to the next higher bet cell means without change;

The BRV of the bit cell means the voltage available on the reference voltage of the reference resistance means for M^{th} cell BRV is equal to system reference voltage divided by 2^M;

adder means the sum of analog input voltage and ½ LSB voltage to minimize quantitized error to ½ LSB;

S&H circuit means to hold the output of said adder output when third switch is activated by the clock means to make available to all comparators for processing;

reference voltage of the system is equal to half of the maximum analog voltage for which the ADC is made;

a common analog signal connected to all comparators;

and plurality of such bit cells means connected in cascade means connecting from most significant bit (MSB) to lowest significant bit (LSB) to provide parallel analog to digital conversion (ADC) of the analog signal means voltage across capacitor of '$M^{th'}$ cell is added to the quantized voltage sensed by $(M+1)^{th}$ cell when the status of M^{th} cell is logical '1' whereas it is not added to the cell $(M+1)^{th}$ if the status of M^{th} cell is logical '0', and the other end of the capacitor of the last cell i.e. MSB it is connected to ground hence quantitized voltages on all bit cells are available with respect to ground which are dependent on the logical state of respective bit cells from MSB to LSB such voltage on M^{th} cell for 'N' stage ADC can be expressed in the form of an equation given by:

$Vd_m=V_{r1}*[Nb*(2)^(N-1)+N(b-1)*(2)^(N-2)+N(b-2)*(2)^(N-2)+…+Mb(N-M)*(2)^(N-M)]$

Where

N>M

'N'= number of bit cells/stages and N-1= next higher bit cell,

Vd_m = voltage on M^{th} bit cell = sum of the binary reference voltages (BRV) at the bit cell including higher bit cells = quantized voltage

V_{r1} = reference voltage of lowest significant bit cell i.e. LSB $=Vr/2^N$ of N bit ADC

Mb = logic state of M^{th} bit cell ie Mb =1 for logic '1' state and Mb=0 for logic '0' state,

means logical state '1' will add and logical '0' will have no effect on quantitized voltage of the plurality of comparator and on the contrary depending upon the inputs to the said comparator if its output does not change means logical state '0' then the output of the lower end of the capacitor of the adjacent lower significant bit cell is directly connected to

one end of the capacitor of the adjacent lower bit cell means bypassing the said capacitor means bit cell BRV thereby logical state '0' of the said bit cell will not affect the quantitized voltage available to the adjacent higher bit cell binary voltage and thus bit binary voltage is added in sequence from most significant bit to least significant bit in series depending upon the logical state of the individual bit cell and whereas the capacitor of MSB is grounded and thus the said plurality of converter stages further being configured to carry out conversion of the analog input signal to a plurality of parallel digital output bits from said converter simultaneously add in a flash manner and further providing quantized output from the least significant bit to most significant bit. As a result, adding additional converter stages to the flash ADC of this invention increases circuit requirement only linearly, rather than exponentially, as in the case of prior art flash ADC. For 'N' bit flash ADC requires one system reference voltage source, N comparators, N reference resistances, 2N+1 switches. The reference voltage available of M^{th} bit cell can be given by the expression:

$$Vm=Vr\left(\frac{1}{2}^{(M+1)}+\frac{1}{2}^{(M+2)}+\frac{1}{2}^{(M+3)}+\ldots+\frac{1}{2}^{(N-1)}+\frac{1}{2}^{(N)}+\frac{1}{2}^{(N)}\right)=Vr\left(\frac{1}{2}^{(M)}\right)$$

Where,

Vr= system reference voltage

Vm=reference voltage on M^{th} bit cell,

$Vr\left(\frac{1}{2}^{(M+1)}\right)$ = reference voltage on next higher bit cell

$Vr\left(\frac{1}{2}^{(N)}\right)$= Vr1=reference voltage on LSB cell

It is apparent from the aforesaid expression that the value of the reference resistance decreases exponentially from MSB to LSB current being the same through all resistances.

The attainment of the foregoing and related objects, advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention, taken together with the drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS:

Sheet 1 of 3 shows FIG. 1 showing a circuit diagram of a typical bit cell i.e. M^{th} of the said capacitor ladder flash ADC, which illustrates the expansion lines in accordance with the invention

Sheet 2 of 3 shows FIG. 2 showing a circuit diagram of synchronous operation of said capacitor ladder flash ADC, which illustrates a typical 3 bit ADC comprising FIG. 1 with provisions for expansion to 'N' bit resolution and for a quantized and ½ LSB error using an adder circuit, output latch, clock in accordance with the invention.

Sheet 3 of 3 shows FIG. 3 showing a circuit diagram of synchronous operation of said capacitor ladder flash ADC, which illustrates a typical 3 bit ADC comprising FIG. 1 and fig. 2 with provisions of reference voltage source for each bit cell.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a schematic diagram a single bit capacitor ladder flash ADC of the present invention. It is a basic bit cell and by cascading such cells any resolution of ADC can be realized. A typical M^{th} bit is described in the following description. It comprises a bit dependent resistances namely reference resistance M5, one comparator M1, two semiconductor switches M2 operated by the comparator M1 and M4 operated by the clock 6 respectively and where the voltage drop on the resistance is equal to $Vr/2^M$ where Vr is the system reference voltage source of ADC circuit. The reference voltage on M5 is connected to capacitor M3 through switch M4. Common analog signal is connected via bus 16 to non-inverting input M6 of the comparator M1. Pole M14 of switch M4, one end M13 of capacitor M3 are connected to inverting input M7 of comparator M1. Comparator M1 output M8 is connected to the control line M9 of the semiconductor switch M2. The output M8 of comparator M1 is taken as output of the bit cell M and connected to output line Mb. One pole of switch M2 and one end of capacitor M2 are connected to bus M12. M12 is a bus going to lower bit cell i.e. (M-1). Common pole of switch M2 is connected to bus M10. M10 is a bus going to higher bit cell i.e. (M+1). Control input 17 of switch M4 is connected to system clock 6. Another pole M15 of switch M4 is connected to reference resistance M5. One end M16 of reference resistance M5 is connected to next lower bit cell while another end M17 of resistance M5 is connected to next higher bit cell (M+1).

Now referring to Fig.2 which comprises N number of bit cells. The MSB cell is described as cell A which is similar to bit cell M except the terminal A12 of capacitor A3 is connected to ground 19 and the value of bit dependent reference resistance is different. Similarly bit cell N is similar to bit cell M except the bit dependent reference resistance end is grounded to 20 and quantitized voltage of ADC is outputted to 18 via bus N10. Analog voltage bus is connected to A6..M6..N6 of bit cell A..M..N

respectively. Reference voltage which is half of maximum analog voltage for which the ADC is designed is connected to the series combination of reference resistances A5..M5..N5 where other end N17 of resistance n5 is grounded to 20. The digital outputs Ab..Mb..Nb of bit cells A..M..N are connected to latch 21. The capacitor N3 end N12 is connected to capacitor M3 end M13 via bus M10 which is in turn connected via M12 to capacitor A3 end A13 via bus A10 which is connected to A12 which is connected to ground 19 thus forming a capacitor ladder. Analog input 1 and ½ LSB voltage 2 are connected to adder 3. Adder 3 output 4 is connected to sample and hold circuit (S&H CKT) 5. Clock 6 output 8 is connected to S&H CKT 5 through control line 7. Clock 6 output 8 is connected to semiconductor switch 15 through control line 17. Clock 6 output 8 is connected to respective control line 17 of semiconductor switches A4...M4..N4 through line 10. Clock 6 output 8 is connected to latch 21 via line 19. When clock is initiated it disables the latch, grounds the common analog signal 16 to non-inverting inputs A6..M6..N6 of comparators A1...M1...N11 and comparator output A8..M8..N8 goes low respectively. The semiconductor switches A2..M2..N2 are deactivated and line A10..M10..N10 is connected to capacitor terminals A12..M12..N12 which in turn is connected to ground 19. The activation of the clock further activates semiconductor switch A4..M4..N4 which in turn connectes capacitor terminal A13..M13..N13 to A15..M15..N15 thus the capacitors get charged to the voltage on reference resistance A5..M5..N5 respectively to their respective BRV. When the clock changes state the semiconductor switches A4..M4..N4 deactivates means get opened and isolates the charged capacitors from the reference resistances respectively. Clock signal further activates S&H CKT and it holds the analog signal. Clock signal further deactivated semiconductor switch 15 and connects common analog signal bus to S&H CKT signal and further latch 21 is activated. Each comparator compares the analog signal with quantitized voltage available on the specific bit. The digital outputs are

available on the output of all comparators with some propagation delay however, in a flash mode.

Referring to Fig.3 shows another embodiment of the said ADC where other circuit remaining same reference resistance A5..M5..N5 and common voltage source 11 as shown in Fig. 2 have been replaced by N independent voltage sources A18..M18..N18 for bit cell A..M..N respectively. The reference voltage Va..Vm..Vn are equal to $Vr/2^{A}..Vr/2^{M}..Vr/2^{N}$ where N>M>A=1 for A..M..N bit cell respectively.

It should further be apparent to those skilled in the art that various changes in form, combination thereof and details of the invention as shown and described may be made to suit particular requirement or requirements.

We Claim:

1. According to this invention the capacitor ladder flash analog to digital converter (ADC) for converting analog input signal into coded binary digital outputs comprising number of bit cells and each bit cell comprising of;

a reference voltage source;

a capacitor means coupled between next lower bit circuit and next higher bit circuit for providing binary reference voltage (BRV) ;

a first semiconductor switch means coupled between one end of capacitor and next lower bit circuit means connecting the capacitor across the respective reference voltage source and ground for providing reference quantitized voltage of the bit cell when first switch is deactivated means 'off' condition and second switch it is closed means 'on' condition;

a comparator means for comparing the input analog signal connected to non-inverting input and quantitized voltage of the bit cell connected to inverting input and controlling the first semiconductor switch means when the analog signal is greater than the quantitized voltage to close the semiconductor switch under digital '1' condition means activated otherwise open the semiconductor switch under digital '0' condition thereby connecting the quantitized voltage of next lower bit section to next higher bit circuit thereby bypassing the capacitor and to further means provide a digital out put of the ADC pertaining to that bit cell;

a voltage reference source means providing voltage proportional to the binary reference voltage (BRV) of the bit cell means voltage drop across the reference resistance;

a third switch means common to all the bit cells of ADC operated by clock circuit means under activated condition by the clock circuit means closed condition connects the common bus of analog voltage to ground and isolated the input analog voltage from the common analog voltage bus of all bit cells; whereas when it is deactivated it connects the input analog signal to the common bus of analog voltage to all bit cells for

ADC operation;

the voltage to the comparator inverting input means the quantitized voltage of the lower bit cells added to the BRV means the reference voltage acroos the capacitor due to the voltage of voltage source of the same bit cell;

the quantitized voltage of the bit cell under closed switch means under digital '1' condition means the binary dependent voltage means the voltage across capacitor and voltage due to the lower significant bits means quantitized voltage of lower significant bet cells is added means BRV added means to the quantitized voltage to the higher bit cells available on the other end of capacitor means to the higher bit cell and means its one terminal connected to the next lower bit cell with added BRV;

the quantitized voltage of the bit cell under deactivated switch condition means under digital '0' condition means the voltage across capacitor is by passed means not added to quantitized voltage of lower bit means directly available to the next higher bet cell means without change;

The BRV of the bit cell means the voltage available on the reference voltage of the reference resistance means for M^{th} cell BRV is equal to system reference voltage divided by 2^M;

adder means the sum of analog input voltage and ½ LSB voltage to minimize quantitized error to ½ LSB;

S&H circuit means to hold the output of said adder output when third switch is activated by the clock means to make available to all comparators for processing;

reference voltage of the system is equal to half of the maximum analog voltage for which the ADC is made;

a common analog signal connected to all comparators;

and plurality of such bit cells means connected in cascade means connecting from most significant bit (MSB) to lowest significant bit (LSB) to provide parallel analog to digital conversion (ADC) of the

analog signal means voltage across capacitor of '$M^{th'}$ cell is added to the quantized voltage sensed by $(M+1)^{th}$ cell when the status of M^{th} cell is logical '1' whereas it is not added to the cell $(M+1)^{th}$ if the status of M^{th} cell is logical '0', and the other end of the capacitor of the last cell i.e. MSB it is connected to ground hence quantitized voltages on all bit cells are available with respect to ground which are dependent on the logical state of respective bit cells from MSB to LSB.

2. ADC of claim 1, wherein the cascading of plurality of bit cells means each bit cell having voltage reference available on reference resistance means binary reference voltage (BRV) equivalent to the corresponding bit cell position means connected in terms of their hierarchy means connecting from most significant bit (MSB) to lowest significant bit (LSB) means.

3 ADC of claim 1, wherein the current source means each bit cell carries different reference voltage equivalent to its position in the hierarchy of the plurality of cascaded bit cells means for M^{th} bit cell reference voltage given by $I/2^M$.

4 ADC in claim 1, wherein reference voltage available on reference resistance include independent voltage source corresponding to BRV.

5 ADC in claim 1, wherein LSB means the bit cell having the least BRV and further the quantitized voltage of ADC available.

6. ADC in claim 1, wherein MSB means the bit cell having the maximum BRV and further one end of capacitor connected to ground.

7. ADC in claim 1, wherein the cascade connection of bit cells means the capacitor of all bits means in series thus forming plurality of capacitor means capacitor ladder.

8. ADC in claim 1, wherein common analog signal means connecting to the comparator inputs of all bit cells of ADC.

9. Analog signal in claim 8 means generally processed by adder, clock, and S&H circuits to minimize conversion error to 1/2 LSB and for a synchronous operation.

10. Parallel binary digital out puts in claim 1 means generally processed by latch, clock circuits and for a synchronous operation.

11. ADC in claim in 1, wherein for asynchronous operation means direct conversion of analog signal means directly connected to comparators input and digital output means directly available on the comparator outputs means with 1 LSB conversion error without adder circuit.

12. ADC as in claim 1 and as recited in claim 2 to 11 and as described and illustrated in preferred embodiments and ascertain the nature of this invention and the manner in which it is to be performed and revealed in diagrams of Fig. 1, Fig. 2, and Fig3.

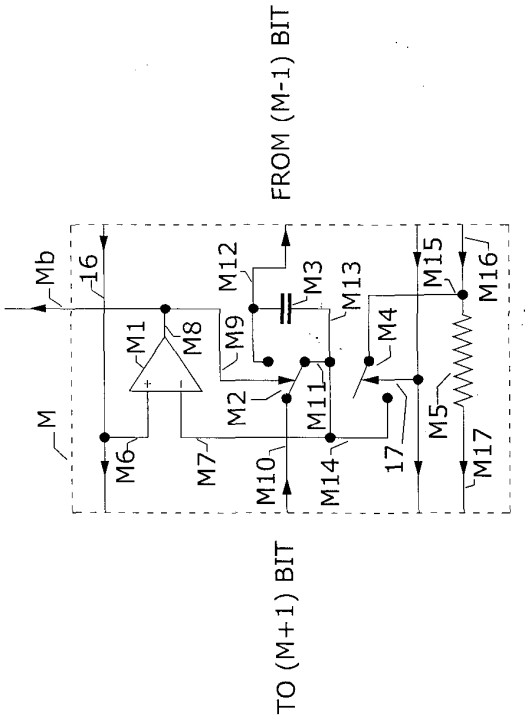
* * * * *

ABSTRACT:-

An analog to digital capacitor ladder flash converter (ADC) is disclosed having a multiple bit, parallel digital output arranged in least significant bit (LSB) to most significant bits (MSB) each comprising a replicated individual stage of bit cell circuit configuration. The resolution of the said ADC depends upon the number of such bit cells. Each replicated bit circuit comprises a single bit having its bit dependent binary weighted voltage, two semiconductor switches, one comparator, and one resistance,. The input analog voltage is connected to a plurality of the said arranged converter stages. The respective comparator in each bit cell compares the input analog voltage with its own binary weighted voltage available on its capacitor added to the bit dependent binary weighted voltage depending upon the respective bit status, known as quantized voltage, of adjacent more significant bit cell. Whereas such voltage is independent of the analog signal input voltage but dependent on the binary state of the adjacent more significant bit cells quantized voltage available on their respective capacitor and supplies to any adjacent lower significant bit cell. Comparators provide parallel digital bit out puts depending upon their respective binary status. The converter converts the analog input signal to digital output bits simultaneously in flash manner. The invention is further revealed in Fig.1 which shows circuit diagram of flash ADC with provision for expansion to 'N' bit resolution in accordance with the invention and further explained by Fig.2, and Fig. 3 .

Multi-cont - Mayak Vijay Tulshiram. Sheet 3/3.

Fig. 1

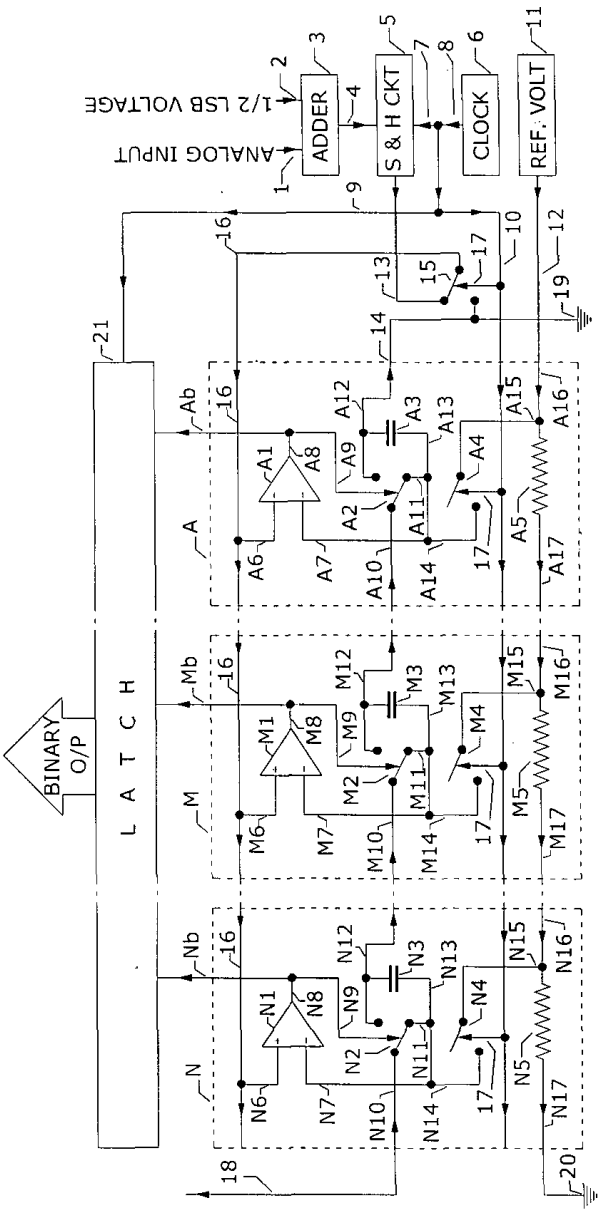


21 DEC 2009

Applicant - Ingole - Vijay Tulshiram.

Sheet 3/2

Fig. 2

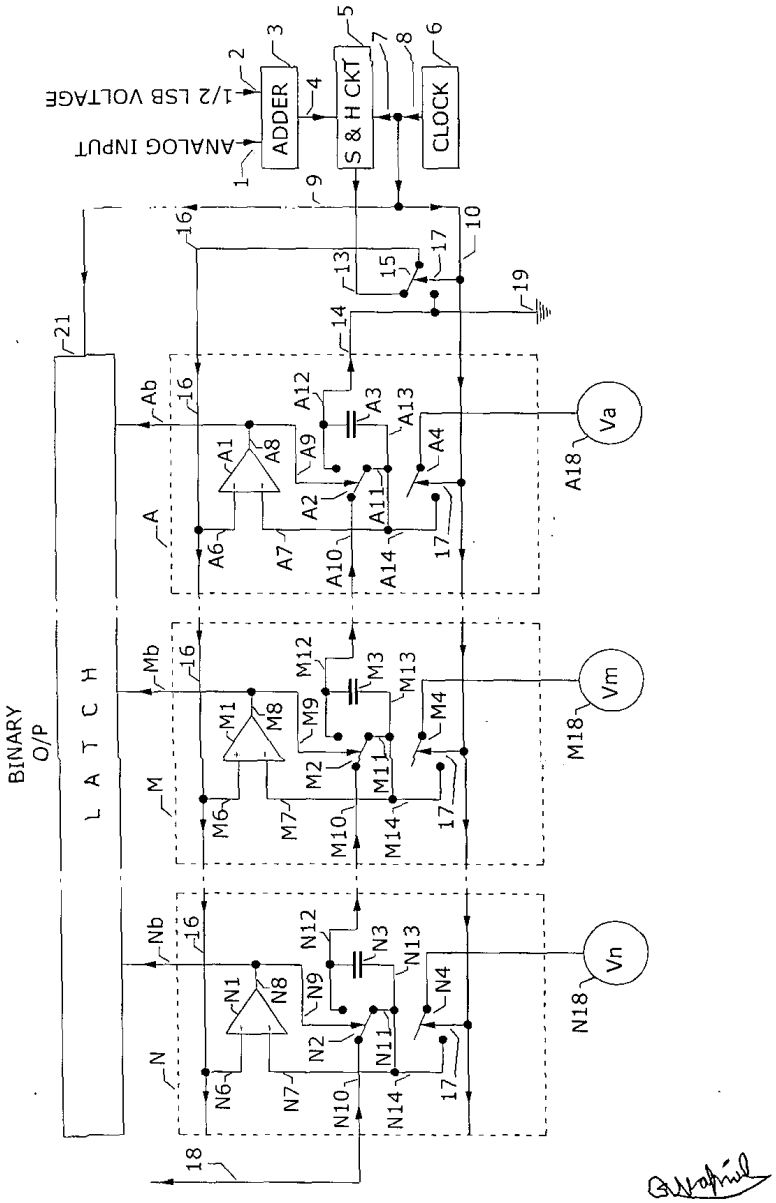


21 DEC 2009

Applicant Ingole - Vijay Nikhilesh

Sheet 3/3.

Fig.3



21 DEC 2009

FORM 3

THE PATENT ACT 1970
(39 OF 1970)
AND
The patent rules, 2003
STATEMENT AND UNDERTAKING UNDER SECTION 8
(See section 8; rule 12)

We

Name	Nationality	Address
Ingole Vijay Tulshiram	Indian	104 Ganediwal layout, camp, Amravati-444602
Ingole Ashutosh Vijay	Indian	104 Ganediwal layout,camp,Amravati-444602
Ingole Paritosh Vijay	Indian	104 Ganediwal layout,camp,Amravati-444602

Hereby declare:-
(i) that we have not made any this application for the same /substantially the same invention outside India.

Dated this 21st day of November 2009

Signature

To
The controller of patents,
The patent office,
At Mumbai.

FORM 9

THE PATENT ACT 1970
(39 OF 1970)
AND
The patent rules, 2003

REQUEST FOR PUBLICATION
(See section 11-A(2);rule24-A)

We

Name	Nationality	Address
Ingole Vijay Tulshiram	Indian	104 Ganediwal layout,camp,Amravati-444602
Ingole Ashutosh Vijay	Indian	104 Ganediwal layout,camp,Amravati-444602
Ingole Paritosh Vijay	Indian	104 Ganediwal layout,camp,Amravati-444602

Hereby request for early publication of our application titled “capacitor ladder flash analog to digital converter” attached herewith the application under section 11(a) 2 of the act.

Dated this 21st day of November 2009

Signature

To
The controller of patents,
The patent office,
At Mumbai.

FORM 18 (FOR OFFICE USE ONLY)

THE PATENT ACT 1970
(39 OF 1970) Application number:
And filing date:
The patent rules, 2003 amount of fee paid:
CBR NO:

REQUEST FOR EXAMINATION OF APPLICATION OF PATENT
[See section 11-B and rules 20(4)(ii),24-B(1)(i)]

1. APPLICANT

Name	Nationality	Address
Ingole Vijay Tulshiram	Indian	104 Ganediwal layout,camp,Amravati-444602
Ingole Ashutosh Vijay	Indian	104 Ganediwal layout,camp,Amravati-444602
Ingole Paritosh Vijay	Indian	104 Ganediwal layout,camp,Amravati-444602

We hereby request that our application for patent titled "capacitor ladder flash analog to digital converter" attached herewith the application shall be examined under section 12 and 13 of the act.

Address for service: - 104 Ganediwal layout, camp, Amravati-444602.

Dated this 21st day of November 2009

Signature

To
The controller of patents,
The patent office,
At Mumbai