Form 2
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(39 OF 1970)
AND
The patent rules, 2003

COMPLETE SPECIFICATION
(See section 10: rule 13)

1. TITLE OF INVENTION

Binary Ternary DAC, ADC

2 APPLICANTS

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3. PREAMBLE TO THE DESCRIPTION

COMPLETE

Following specification particularly describes the invention and the manner in which it is to be performed.

DESCRIPTION:-

1. FIELD OF THE INVENTION:

This invention generally relates to Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) for Multi Value Digital Logic including Binary Digit logic system which are also compatible with each other for digital to digital conversion (DDC) and; particularly applicable to Binary and Ternary Digital logic systems. Due to the advent of multi value Digital logic (MVL) particularly Ternary digital system, in Digital Processors it has become imperative to have input/output interface for the compatibility of such systems for combined functioning, for conversion of data from any radix digit system to any other radix digital system and further for their peripheral interfaces. Further such ADC, DAC converters also function independently for the signal processing thereof.

2. BACKGROUND OF INVENTION:

Following invention comprises said DAC, ADC, and combinations their off for DDC and further having fast conversion speed, low component count, simple topology, high package density, and simple layout, compatible with latest state of art in manufacturing.

Prior Art:

Integrated circuit topologies for ADC/DAC have been reported in the prior art:

Flash ADC with n-bit resolution require $(2^n - 1)$ comparators. The necessity to provide such large numbers of comparators limited their applications and Pipeline topology using multiple flash ADC for limited digit number ensued however, at the cost of complexity. Quite a few improvements in flash ADC design have been reported having reduced number of comparators per bit output but they still suffers from the

much higher component count, large number of current buses, high current requirement and circuit complexity.

Conventional Sequential Approximation Register (SAR) type ADC employs SAR logic and requires number of conversion clock pulses depending on the number of digits involving unnecessary iteration clock cycles rendering them slow in conversion rate. Whereas Time Interleaved ADC employs number of buffer circuits however, has nonlinear response and introduces distortion to the input signal particularly for high speed ADC operation with low supply voltage.

Adaptive ternary A/D converter for use in an ultra-wideband communication system an US Patent 8,436,759 B2, Dated May 7, 2013 reportedly used SAR logic employing signal routed through buffers and comparators to minimize distortions and to reduce nonlinearity however, requires calibration of feedback DAC however, appears to be complex and suffer from the inherent speed limitation of SAR logic ADC.

US Patent 8,188,902 B1, Dated May 29, 2012 reported used Ternary search algorithm instead of binary search algorithm in SAR logic to reduce number of switching event to save power however, appears to be complex and suffer from the inherent speed limitation of SAR logic ADC.

US Patent 7,936,2979 B2, Dated May 37, 2011 reported used an residue amplifier between the bandwidth voltage of two successive N and N+1 digits and low pass filter however, appears to be complex and suffer from the inherent speed limitation of SAR logic ADC.

Differential input successive approximation analog to digital converter with common mode rejection is mentioned in US 20080129573 A1, dated 5 June 2008. A Successive Approximation Routine converter is provided in which a comparator is responsive to an output of a first

Digital to Analog Converter, and an output of a second Digital to Analog Converter and to a DAC common mode output reference voltage, and wherein the comparator provides data to a SAR controller indicating which one of the DAC outputs is greater than the other, and how a common mode voltage on the DAC outputs compares to the reference voltage. On this basis the SAR controller can add or subtract a common mode offset to the trial words being presented at a given bit trial such that both differential and common mode convergence is achieved.

US Patent 6,958,722 B1, Dated Oct. 25, 2005 reported used two additional comparator buffers to improve the accuracy of conversion and appears to be complex and suffer from the inherent speed limitation of SAR logic ADC.

DACs have been reported such as:

US Patent 8,410,966 B2, Dated Feb. 2, 2013 employing current DAC having switchable resistance network with feedback, FET devices and appears to be complex, high in device count.

As regards Ternary DAC and Ternary ADC not much literature is available.

Another Digital to analog converter (DAC) with ternary or tri-state current source is described in US 8471745 B2, dated 25 June 2013.

A DAC including a number of ternary or tri-state devices operates based upon code words provided thereto. Generally, each respective code word bit directs operation of one of the respective ternary or tri-state devices within the DAC. Each ternary or tri-state device operates in at least three respective operational states (e.g., based upon the respective values of +1, −1, or 0 being provided thereto). In a current source implementation, each respective current source is implemented to deliver current, draw current, or neither delivered or draw current. In a voltage source

implementation, each respective voltage source is implemented to provide a positive voltage, a negative voltage, or provide no voltage. A DAC coding table may be designed based upon characterization of code words provided to one or more DACs (e.g., based upon a distribution, a probability density function (PDF), etc. of such code words).

In summary, from the prior art ADC, DAC appear to suffer either from large number of devices as in flash ADC or circuit complexity, slow speed as in case of SAR and Analog to Digital Converter (ADC) employs resistance ladder net work though being the simplest, suffers from resistance matching and power consumption and further it can be said that most of the converters suffer from complexity, high device count, lower conversion speed hence a necessity is felt for a high speed binary and MVL digital ADC, DAC which are also compatible with each other for their combined operation for digital to digital conversion (DDC) and further which are simple in design, having low component count, low power consumption, and simplicity in design and layout, enhance resolution and easily implemented in present day VLSI fabrication technology.

Object:

1. A primary object of the present invention is to provide a novel ADC and DAC topology which have faster conversion rate;
2. Another object of the present invention is to provide a parallel ADC and DAC for single clock cycle conversion;
3. Another object of the present invention is to provide a parallel ADC and DAC functioning and avoiding superfluous approximation attempts during conversion;

4. Further objective of the present invention is to provide ADC which has comparable conversion rate that of flash ADC but having limited number of comparator devices;

5. Still further objective of the present invention is to provide ADC and DAC which have lower power requirement and having eliminated resistive elements;

6. Further objective of the present invention is to provide ADC and DAC which have simple circuit topology with very low component count;

7. Further objective of the present invention is to provide ADC and DAC which have low device count;

8. Further objective of the present invention is to provide ADC and DAC which have plurality of said circuits being similar in nature for ease of fabrication and higher package density;

9. Further objective of the present invention is to provide ADC and DAC which have simple conversion logic and compatibility;

10. Further objective of the present invention is to provide quantized output of ADC is inbuilt in the circuit topology;

11. It is a still further objective of the invention to provide ADC and ADC having minimum voltage/current buses and interconnections;

12. It is a still further objective of the invention to provide reference sources being restored every clock cycle to minimize conversion error;

Further objects and features can be readily understood by any person skilled in the art by referring to the detail description and appended claims of the invention.

STATEMENT:

The attainment of the foregoing and related objects are achieved through use of the novel charged reference capacitor topology herein disclosed and according to this invention ADC and DAC comprising plurality of digit cells and each said cell comprising one of the first embodiment hereinafter referred to as register having a reference voltage source pertaining to respective digital level means hierarchical order; a capacitor meant for storing reference voltage charge of respective digital cell; and the said reference voltage being stored on the capacitor and is restored by every clock cycle to minimize conversion error, preferably when the clock signal is low; and plurality of such replicated digit-wise, means in respective hierarchical order, charged capacitors sequentially arranged from lowest significant digit (LSD) to highest significant digit (HSD) having a common clock so as to operate in parallel; and the digit reference voltage stored on the said capacitor being equal to $v_r=n*v_q*m^r$ where v_q being quantized voltage where n>0, digit reference voltage (DRV) for lowest significant digit, n= digit number value between 1 and (r-1), r = radix or base, m= position of digit or order means hierarchy for example in ternary logic system for m^{th} digit and for v_q =0.02 volt (assumed), n=2 (digit value), r=3 (radix), m= 4 (position means order oe hierarchy) then respective digit voltage v_r=2*0.02*4^3= 3.24 volts however, for n=0 digit value reference capacitor isolated means disconnected ; and the said capacitor with associated logic circuit forms a register of m^{th} order and said register is connected to receive voltage from higher digit register $(m+1)_1^{th}$ and connected to lower order digit register $(m-1)_n^{th}$ to provide voltage for further operation; and first plate of the said capacitor is connected to said reference voltage through a normally closed contact of single pole single throw switch S1 and remaining plate means second plate of the capacitor is connected to

normally closed contact of single pole double throw switch S2 and further connected to the common contact of similar switch S2 of the next higher digit register which is finally connected to ground voltage through the common contact of similar switch of the highest order register wherein the final ground termination is provided at the MSD register; and the common contact of the switch S2 is connected normally closed contact of similar switch S2 of the next lower digit register; normally open contact of S2 switch is connected the first plate of the said capacitor; and when the switch S1 is deactivated by system clock, preferably when the clock signal is low, whilst the first plate of said capacitor and similar capacitors of all cells, are connected concurrently to respective digit reference voltages through S1 and the second plate of the said capacitor, and similar capacitors of all cells are connected to ground through the normally closed contact of switch S2, and similar switches of all cells, so as to get the respective capacitors charged to respective digit reference voltages; and when the control signal in the clock cycle is high the switch S1 is activated and disconnects first plate of capacitors of all respective cells, being charged to corresponding digit reference voltages, from the reference voltage source; the switch S2 is activated by double pole single throw switch S3 of the said register and the common contact is connected to control the operation of said switch S2, normally closed contact is connected to ground and normally open contact is connected to the output of remaining embodiment of the said digit cell and the said switch S3 is configured in such a manner that when it is deactivated by system negative clock cycle , it deactivates said switch S2 and when switch S3 is activated by system positive clock cycle the normally open terminal of the switch is connected to output of other embodiment of the digit cell and if the said output is high and switch S3 in active condition, switch S2 is activated and thereupon the

common contact of switch S2 is connected to the first plate of capacitor and adds the respective cell reference voltage to the input voltage of higher digit cell and provides the said summed voltage to the lower digit cell for further operation, however, if the said output of digit cell is low and switch S3 in active condition, switch S2 is deactivated and thereupon the common contact of switch S2 is connected to the second plate of capacitor which in turn connects the higher digit register directly to lower digit register thereby bypassing the capacitor means the reference voltage thereupon, of the said register and voltage from the higher digit cell directly connected to the lower digit registers and used for further functioning of corresponding digit cell; and if input to switch S3 is taken as 'x' having value either '1' or '0' the quantized voltage of all m registers, where m=1 to m, can be expressed as summation of digit reference voltage of all m registers: $Vqm=\sum x*n*v_q*m^r$; and other embodiment of the present invention comprises DAC where the digit voltage of m^{th} order is connected to the input of switch S3 of m^{th} register and the analog output voltage Vdac of the m digit operand is outputted voltage at normally open contact of switch S2 of LSD register and further the voltage of the register at any digit outputs the analog conversion of the higher significant digits connected to the said register and given by equation $Van=\sum x*n*v_q*m^r$, where x denotes the respective digit level, either 1 or 0, thus in one clock cycle for negative going pulse all capacitors are charge to their respective significant digits and during positive going cycle digital to analog conversion is completed ; and another embodiment for ADC operation comprises a comparator of which non inverting input of all comparators of the respective digit cell are connected to the analog input, under digital conversion, and inverting input is connected to the respective register output voltage of plurality of digit cells of the first embodiment

and if the analog input is higher than the respective register voltage then the comparator output will go high which represent digital output '1' of the respective digit cell being outputted and further operates the first embodiment where the digit reference voltage is added to the digit reference voltage of higher digit register and connected to lower digit registers for comparison by respective comparators whereas if the analog input is lower than the respective register voltage then digit reference voltage then the comparator output will go low which represents' digital output '0' being outputted and further operates the first embodiment thereby bypassing the respective register voltage means the said register does not influence the lower register voltages and the said process is completed in positive going pulse of the clock cycle till $Van=\sum x*n*v_q*m^r$, where x denotes the respective comparator level, means for high output=1, low output=0 and Van= input analog signal; further the input analog signal may be processed and passed through sample and hold circuit as described in the prior arts; and further the said ADC and DAC converters may work as an independent converter or combination thereof for converting DATA or Addresses of any particular type of digital system to any other type of digital system meant for processing;

The attainment of the foregoing and related objects, advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention, taken together with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS:

Though the embodiments of the present invention so described are applicable to multi value logic systems including binary logic, the present description is described for binary, ternary logic systems

particularly for their interfacing for any desired processing applications and digital to digital data conversion:

Figure-1 of sheet 1 showing a signal flow block diagram 140 of 'n' radix digital system for convection to 'm' radix digital system for their interface and back to 'n' radix digital system where block 141 denotes the 'n' radix digital data input, block **142** denotes digital to digital converter of 'n' radix digital data to 'm' radix digital data, block **143** denotes 'm' radix digital processing system, block **144** denotes digital to digital converter of 'm' radix digital data to 'n' radix digital data, block **145** denotes 'n' digit system processed data.

Figure- 2 of sheet 1 showing a signal flow block diagram **150** for binary digital system for convection to ternary digital system interface and back to binary digital system interface where block **151** denotes binary digital data input, block **152** denotes binary digital to analog conversion(DAC), block **153** denotes analog to ternary digital converter (ADC), block **154** denotes ternary digital system processor, block **155** denotes ternary digital to analog converter (DAC), block **156** denotes analog to binary digital converter (ADC) and block **157** shows processed binary data.

Figure- 3 of sheet 1 showing a signal flow block diagram 160 for binary digital system for convection to ternary digital system interface and back to binary digital system in details with system clock **950** where block **161** denotes binary digital register input, block **162** denotes binary digital to analog conversion (DAC) **350**, block **163** denotes analog to ternary digital converter (ADC) **950**, block **164** denotes temporary latch for ternary data, **165** denotes ternary digital system processor, block 166 denotes ternary digital to analog converter (DAC) **350**, block **167** denotes analog to binary digital converter (ADC) **950**, block **168** denotes temporary latch for binary data and block **157** shows processed binary data register for further processing.

Sheet 2 of 4: Figure- 4 shows the schematic block diagram **100** of the topology of the present invention where block **130** denotes Digital to Analog conversion (DAC) comprising block **135** for digital data input **136**, block **131** for analog signal output **132**, selection switches **134**, **137**,; block **120** denotes Analog to Digital conversion (ADC) comprising block **125** for analog input **122**, block **121** for digital output **122**, comparator **128** and selection switches **124, 124, 126, 127;** quantized voltage block **110** comprising quantized digit reference voltage block **114**, connected to either block **130** or **120** through switches and further connected to lower significant quantized voltage block **116** and higher significant quantized voltage block **111**.

Sheet 3 of 4: Figure-5 shows the schematic diagram of a binary DAC digit cell; Figure-6 shows the circuit diagram of a DAC digit cell; Figure-7 shows the block diagram of DAC digit cell Figure-8 shows the plurality of DAC digit cell in series for parallel operation.

Sheet 4 of 4: Figure-9 shows the schematic diagram of a ternary ADC digit cell; Figure-10 shows the circuit diagram of a ternary ADC digit cell; Figure-11 shows the block diagram of ternary ADC digit cell Figure-12 shows the plurality of ternary ADC digit cell in series for parallel operation

DETAILED DESCRIPTION OF THE INVENTION:-

Figure 1 of sheet 1 showing a signal flow block diagram **140** to interface two MVL digital systems where, in block **141** digital data of ‘n’ radix digit system is retrieved and provided to block **142** for digital to digital conversion (DDC) form ‘n’ radix system to ‘m’ radix digital system and such digital to digital converted (DDC) signal is provided to ‘m’ radix processor of block **143** and after due processing therein, the output

digital signal of 'm' radix system converted back to digital signal of 'n' radix system by digital to digital converter (DDC) in block 144 and such reconverted signal data outputted to block **145** for further processing.

Figure 2 of sheet 1 showing a signal flow block diagram **150** for a typical binary digital system data to be converted to another typical ternary digital system processor and reconverting such ternary system data back to binary digital system where, in block **151** binary digital system data is retrieved and provided to block **152** for digital to analog conversion (DAC) and such analog signal is provided to block **153** for analog to digital conversion (ADC) to the said ternary digital system and the said digital data is provided to ternary processor in block **154** and the such processed ternary digital data is provided to block **155** to be converted to analog signal by DAC and the said analog signal is provided to block **156** to be converted to binary digital system by ADC and such reconverted binary signal data outputted to block **157** for further processing.

Figure 3 of sheet 1 showing a signal flow block diagram **160** for a typical binary digital system data to be converted to another typical ternary digital system processor described henceforth where block **161** comprises binary data registers inputted to block **162** comprising DAC **361** and output of **361** is inputted to block **162** comprising DAC **350** for analog conversion and output of **162** is inputted to block **163** comprising ADC for digital conversion to ternary digital system and the digital data is inputted to block **164** comprising temporary latch which is retrieved by block **165** comprising ternary digital processor and after due processing the results are inputted to block **166** comprising ternary digital to analog converter and such analog signal is inputted to block **167** comprising analog to binary digital converter and said binary data is inputted to block **168** comprising temporary latch and block **169**

comprises converted binary data retrieved from block 168 for further processing.

Sheet 2 of 4 wherein Figure-4 shows first embodiment block **100** indicating schematic diagram of the basic conversion block (BCB) **110** common to ADC or DAC conversion comprising quantized voltage block (QVB) comprising digit reference voltage block **111** connected to through next higher QVB to plural digit BCB to receive conversion signal **113** from all higher plural BCB **111** and the output **115** of the BCB **114** is inputted through next lower QVB to plural digit BCB **116**. Digit reference voltage block **114** is controlled by control signal input **118** in such a manner that when **118** is high it adds its respective digital reference voltage **114** to voltage **113** received from said BCB **111** and inputs the modified voltage **115** to next said lower BCB **116** whereas when the control signal input **118** is low it bypasses its respective digital reference voltage **114** and inputs voltage **113** received from said higher digit BCB **111** through **115** to plurality of next lower digit BCB **116**. The output **115** thus is the cumulative sum of signals in the form of quantized analog output of the plurality of all higher digits BCB connected to BCB **114**. Analog to digital conversion (ADC) is carried out by second embodiment **120** wherein processed analog signal **128** is received from analog input block **126** and given through selection switch **123** , preferably, to the non-inverting input of a comparator **128** circuit, and inverting input **129** of the said comparator **128** is connected through a selector switch **124** to quantized output **115** and the comparator **128** output is connected through a selector switch **126** to **118** for the operation of first embodiment **110** and further connected through switch **127** and input **122** to digital output block **121**, preferably an encoder, for digital signal processing; and digital to analog conversion (DAC) is carried out by third embodiment **130** wherein processed

decoded digital signal **136** is received from digital input block **135**, preferably a decoder, and connected through selection switch **137** to **118** for the operation of first embodiment **110** and if the level of the digit is high it adds its respective digital reference voltage **114** to voltage **113** received from said BCB **111** and inputs the modified voltage **115** to next said lower BCB **116** whereas when input **118** is low it bypasses its respective digital reference voltage **114** and inputs voltage **113** received from said higher digit BCB **111** through **115** to plurality of next lower digit BCB **116** and LSD digit cell (not shown) **132** is outputted to analog output block **131**. When first embodiment **114** is connected to second embodiment **130** through switches **134** and **137**, the said combination works as a ADC whereas when first embodiment **130** is connected to third embodiment **120** through switches **123**, **124**, **126**, and **127** , the said combination works as DAC.

Sheet 3 of 4 wherein Figure-5 shows the schematic circuit of digit cell **301** for DAC where the plurality of such digit cells in series comprises multi input DAC to execute the conversion in parallel. The respective digit **200** in connected to decoder **235** and decoded input **228** is connected to normally open contact **225** of single pole double throw switch **225**, normally closed contact **223** is connected to ground **293** and common contact **222** is connected to control input **203** of single pole double throw switch **221**, whereas the switch **221** is controlled, means switch **ON**, by the high input signal on **203** and the common contact **220** of the said switch **221** is connected to the normally closed contact **320** next lower digit cell switch **321** and capacitor second plate **316** of the string of the plurality of lower digit cells (not shown) accordingly, and the normally open contact **215** is connected to first plate of capacitor **214** and normally closed contact is connected to second plate of the capacitor **214** except in most significant digit cell, where the second plate of the

similar capacitor is connected to ground **293**, and is further connected to common contact **241** of similar switch **241** of the next higher digit cell of the string of the plurality of digit cells, and the normally open contact **215** is further connected to common contact **212** of single pole single throw switch **213** and the normally closed contact **201** is connected to respective digit reference voltage source (not shown), whereas the switch **213** is controlled, means switches **ON** by the positive going system clock signal **295** and isolates the capacitor **214** from the respective digital reference voltage source (not shown) and in the said manner, only when the respective digit **208** is high the corresponding digit reference voltage present on capacitor **214** is added to the string of plurality of cell voltage otherwise not.

Figure-6 illustrates the preferred circuit topology **302** of a typical digit cell, where **213** represents a single pole singe throw switch and digit reference voltage source (not shown) is connected through **201** to Transmission Gate (TG) **212**. Other terminal **202** of said TG is connected to first plate of capacitor **214**. Positive control gate of said TG is connected to positive bus **291** and negative control gate is connected to system clock input **294**. Combination of TG **215** and TG **216** forms a single pole double throw switch **221** where TG **215** is connected to first plate of capacitor **214** and TG **216** is connected to second plate of capacitor **214** and **229** where **229** is connected to next higher digit cell and remaining terminals of TG **215** & **216** are connected in parallel **219** and further connected to second plate of capacitor of next lower digit cell (not shown). Negative gate of TG **215** is connected to ground **293** and positive gate of TG **216** is connected to positive supply **291** whereas positive gate of TG **215** and negative gate of TG **216** are connected to parallel connection of TG **223** and TG **224**, where the said combination forms a single pole double throw switch **225** and remaining terminal of

TG **223** is connected to ground **293** and remaining terminal of TG **224** is connected to digital input **228** derived from decoder (not shown). The negative gate of TG **223** and positive gate of TG **224** are connected to clock input **294** whereas positive gate of TG **223** is connected to positive supply **291** and negative gate of TG **224** is connected to ground **293** and charges capacitor **214** and plurality of capacitors to their respective digit reference voltages from plurality of digit cells. When clock signal is going through negative phase TG **212** and TG **223** are in **ON** mode and connects **203** to ground **293** and in effect TG **221** is in **ON** mode while rest of TGs is in **OFF** mode, being applicable to plurality of digit cells in said embodiments and the first plate of said capacitor **214** is connected through **201** to respective digit reference voltage (not shown) and second plate of the said capacitor is connected to plurality of similar TG **226** of higher digit cells and further to ground **293** at the maximum significant digit (MSD) **246** (Figure-5). When clock signal is going through positive phase TG **212** is in OFF mode whence **201** isolates capacitor **214** from the respective digit reference voltage source (not shown) and TG **223** is in **OFF** mode, TG **224** is in **ON** mode and connects digital input **228** to **203** for the operation of switch **221**. When the said digital input is high TG **226** becomes **OFF** and TG **225** becomes **ON** and capacitor reference voltage on capacitor **214** is added to voltage at **229** and the said addition of voltages on **229** is passed on to next lower digit cell for DAC conversion, whereas when the said digital input **228** is low **203** becomes low, TG **215** becomes **OFF** and TG **216** becomes **ON** and the input **229** from plurality of higher digit cells is directly connected to **219**, bypassing capacitor **214**, to plurality of next lower digit cells. Thus when Digital Input **228** is high, respective digit reference voltage is added to higher digit voltage otherwise not and the said voltage is connected to lower digit cell and the resultant output is

available at the least significant digit switch **321** thus digital to analog conversion is accomplished and in the said manner, only when the respective digit **208** is high the corresponding digit reference voltage present on capacitor **214** is added to the string of plurality of cell voltage otherwise not.

Figure-7 illustrates a single digit block diagram **300** of the embodiments as described in Figure-5 and Figure-6 and further denoting the respective inputs and outputs connections by respective numbers expressed therein.

Figure-8 shows block **350** wherein the connections of block **300** as illustrated in Figure-7 to form a plurality of digit cells to form a string of DAC block **350** from least significant digit (LSD) to most significant digit (MSD), with their respective digital inputs **200, 400…600** and respective reference voltage inputs **201**, **401…601** connected to their respective digit reference voltages (not shown), and the summation of resultant analog output on **219** of LSD with respect to grounding connection **310** of capacitor second plate **229** of MSD and in the said manner, only when the said respective digital input is high the corresponding digit reference voltage present on said capacitor(s) is added to the string of plurality of cell voltage otherwise not for the conversion of digital to analog conversion.

Sheet 4 of 4 wherein Figure- 9 shows the schematic circuit of digit cell **901** for ADC where the plurality of such digit cells in series comprises multi input ADC to execute the conversion in parallel. The analog input signal **896** is connected to non-inverting input of comparator **827**, output **826** of the said comparator is connected to normally open contact **824** of single pole double throw switch **825**, normally closed contact **823** is connected to ground **893** and common contact **822** is connected to control input **803** of single pole double throw switch **821**, whereas the

said switch **821** is controlled, means switch **ON**, by the high input signal on **803** and the common contact **820** of the said switch **821** is connected to second plate **716** of the next lower digit cell capacitor (not shown) accordingly, and the normally open contact **815** is connected to first plate of capacitor **814** and normally closed contact is connected to second plate of the capacitor **814** except in most significant digit cell, where the second plate of the similar capacitor is connected to ground, and is further connected to common contact **841** of similar switch **841** of the next higher digit cell, and the normally open contact **815** is further connected to common contact **812** of single pole single throw switch **813** and the normally closed contact **801** is connected to respective digit reference voltage source (not shown), whereas the switch 813 switches **ON** by the positive going system clock signal **895** and isolates the capacitor **814** from the respective digital reference voltage source (not shown). The first plate **802** of capacitor **814** is connected to inverting input of comparator **827**. Thus when comparator output **826** is high, respective digit reference voltage is added to higher digit voltage otherwise not and the said voltage is connected to lower digit cell and the resultant output is available at the least significant digit switch **821** as quantized analog output of all digit cells string. Comparator **827** compares the analog input **896** with quantized analog, being logical summation of all higher digit cell string, and if it is lower than summation of voltages on **829** & **814** then its output is low else it is high and the respective digit voltage of lower digit cells added to the said string voltage for further operation so that the quantized output at the LSD and input analog signal are within error limit set and in the said manner, only when the respective comparator output is high the corresponding digit reference voltage present on capacitor **814** is added

otherwise voltage on **814** is not added to the string of plurality of cell quantized voltage for further comparison .

Figure-10 illustrates the preferred circuit topology **902** of a typical digit cell, where **813** represents a single pole singe throw switch and digit reference voltage source (not shown) is connected through **801** to Transmission Gate (TG) **812**. Other terminal of said TG **802** is connected to first plate of capacitor **814**. Positive control gate of said TG **802** is connected to positive bus **891** and negative control gate is connected to system clock input **894**. Combination of TG **815** and TG **816** forms a single pole double throw switch **821** where TG **815** is connected to first plate of capacitor **814** and TG **816** is connected to second plate of capacitor **814** and **829** where **829** is connected to next higher digit cell and remaining terminals of TG **815** & TG **816** are connected in parallel at **809** and further connected to second plate of capacitor of next lower digit cell (not shown). Negative gate of TG **815** is connected to ground **893** and positive gate of TG **816** is connected to positive supply **891** whereas positive gate of TG **815** and negative gate of TG **816** are connected to parallel connection of TG **823** and TG **824**, where the said combination forms a single pole double throw switch 825 and one terminal of TG **824** is connected to output **826** of comparator **827** and remaining terminal is connected to output terminal **828** whereas negative gate is connected to ground **893** and positive gate is connected to system clock input **894**. One terminal of TG **823** is connected to ground **893** and remaining terminal is connected to output terminal **828** whereas positive gate is connected to positive supply **891** and negative gate is connected to system clock input **894**. The non-inverting input of comparator **817** is connected to analog input **896** whereas inverting input is connected to first plate **802** of capacitor **824** having logical summation of quantized voltage of all higher digit reference voltage.

When clock signal is going through negative phase TG **812** and TG **823** are in **ON** mode and connects **803** to ground **893** and in effect TG **821** is in **ON** mode while rest of TGs are in **OFF** mode which also being applicable to plurality of digit cells in said embodiments and the first plate of said capacitor **814** is connected through **801** to respective digit reference voltage (not shown) and second plate of the said capacitor is connected to plurality of similar TG **816** of higher digit cells and further to ground **893** at the maximum significant digit (MSD) **846** (Figure-9). When clock signal is going through positive phase TG **812** is in **OFF** mode whence **801** isolates capacitor **814** from the respective digit reference voltage source (not shown) and TG **823** is in **OFF** mode, TG **824** is in ON mode and connects comparator **817** output **826** to **803** for the operation of switch **821**. When the said output **826** is high TG **826** becomes **OFF** and TG **825** becomes **ON** and capacitor reference voltage on capacitor **814** is added to voltage at **829** and the said addition of voltages on **809** is passed on to next lower digit cell for quantized analog conversion (QAC), whereas when the said digital output **826** is low, **803** becomes low, TG **815** becomes **OFF** and TG **816** becomes **ON** and the input **829** from plurality of higher digit cells is directly connected to **809**, bypassing capacitor **814**, to plurality of next lower digit cells. Thus when comparator output **826** is high, respective digit reference voltage is added to higher digit voltage otherwise not and the said voltage is connected to lower digit cell and the resultant output is available at the least significant digit switch **721** as quantized analog output of all digit cells string. Comparator **817** compares the analog input **896** with quantized analog, being logical summation of all higher digit cell string, and if it is lower than summation of **829** & **814** then its output is low else it is high and the respective digit voltage of lower digit cells added to the said string voltage for further operation so that the quantized

output at the LSD and input analog signal are within error limit set and in the said manner, only when the respective comparator output is high the corresponding digit reference voltage present on capacitor **814** is added otherwise voltage on **814** is not added to the string of plurality of cell quantized voltage for further comparison .

Figure-11 illustrates a single digit block diagram **900** of the embodiments as described in Figure-9 and Figure-10 and further denoting the respective inputs and outputs connections by respective numbers therein.

Figure-12 shows block **950** wherein the connections of block **900** as illustrated in Figure-11 to form a plurality of replicated digit cells to form a string of ADC block **950** from least significant digit (LSD) to most significant digit (MSD), with their respective digital outputs **800, 900…1030** and respective digit reference voltage inputs **801, 901…1031** connected to their respective digit reference voltages, and the summation of resultant quantized analog output on **809** of LSD with respect to grounding connection **992** of capacitor second plate **869** of MSD and in the said manner, only when the said respective digital input is high the corresponding digit reference voltage present on said capacitor(s) is added to the string of plurality of cell voltage otherwise not and the respective digit voltage of lower digit cells added to the said string voltage for further operation so that the quantized output at the LSD and input analog signal are within error limit set and in the said manner, for the comparison by respective comparator with input analog signal for analog to digital conversion.

It should further be apparent to those skilled in the art that various changes in form, combination thereof and details of the invention as shown and described may be made to suit particular requirement or requirements.

CLAIMS

We Claim:

1. A digital to analog converter (DAC), analog to digital converter (ADC) and the combinations their off for digital to digital conversion (DDC) being essential part of electronic computation and processing machines having different radix means multi value logic including binary systems their interface and processing and further comprising:

a. a plurality of replicated circuit combination means digit cell, connected in series and operated by a single clock for their parallel operation and comprising;

b. a first embodiment comprising an n^{th} digit cell capacitor where its first terminal connected through a selector switch to an n^{th} reference voltage source and to maintain the said weighted reference voltage for each successive timing cycle switched periodically means in each cycle and capacitors remaining terminals concurrently connected through other single pole double throw switch (SPDP) of the plurality of replicated digit cells preferably to a ground source to receive the respective charge from respective digit weighted reference voltages, and first terminal of the said capacitor connected through the said SPDP switches of $(n-1)^{th}$ digit cell whereas the said remaining terminal of the said capacitor connected to similar combined switches of $(n+1)^{th}$ digit cell of the plurality of digit cells and the said SPDP switch operated by a control signal during remaining part of the clock signal such that when the said control signal is low the voltage on $(n+1)^{th}$ digit cell quantized voltage directly connected to $(n-1)^{th}$ digit cell whereas when the said control signal is high, the said capacitor of n^{th} cell is connected in between $(n-1)^{th}$ and $(n+1)^{th}$ cell thereby adding the said weighted reference voltage therein and the quantized voltage present on the first

terminal of the said capacitor represents the summation of all higher significant digit cells including the said digit cell and further in the most significant digit (MSD) cell remaining terminal the similar capacitor being at ground voltage, and all plurality of digit cells of the present embodiment connected in series and the voltage of the first terminal of similar capacitor of least significant digit (LSD) cell represents the sum total of quantized voltage of all plurality of digit cells with respect to the status means weight of said control voltages of each digit cell and combination their off and the said control signals are derived from respective digit cells of other embodiments of the present invention;

c. and for digital to analog conversion (DAC) a third embodiment connected to said first embodiment and the third embodiment of the present invention comprises a second SPDP switch connected to as control signal terminal of n^{th} digit cell of said first embodiment, and first terminal of the said second SPDP switch connected to ground whereas second terminal of the said second SPDP switch connected n^{th} input digit source and the first embodiment functions as per the status means weight of the n^{th} digit and the digital to analog conversion (ADC) outputted at first terminal of said LSD cell capacitor and the said conversion process completed in one clock cycle.

d. and for analog to digital conversion (ADC) second embodiment connected to said first embodiment and the second embodiment of the present invention comprises a comparator and one input, preferably non-inverting, connected to an analog signal, being common to all plurality of digit cells, and second input, preferably inverting, connected to the said quantized voltage at the first capacitor of the

said first embodiment of the said digit cell and the output connected to the said control input of the said first embodiment and if the said analog signal becomes greater than said quantized voltage, the comparator output means the said control input becomes high else low and said first embodiment functions accordingly and further the said comparator output outputted as digital output of the said ADC, and similar action executed at all plurality of digit cells and the said quantized output becomes equal to analog input signal within preferably ½ LSD limit and the said conversion process completed in one clock cycle.

2. DAC operation achieved by combination of embodiment three and embodiment one, as claimed in claim 1 for plurality of digits equal to plurality of digit cells in single clock cycle.
3. ADC operation achieved by combination of embodiment two and embodiment one, as claimed in claim 1 for analog signal converting to plurality of digits having equal plurality of digit cells in single clock cycle.
4. Digital to digital conversion (DDC) operation achieved by combination of DAC and ADC as claimed in claim 1,2, and 3 for digital system of any radix to another digital system with different radix.
5. The said capacitor(s) weighted reference voltage means quantized voltage, as claimed in claim 1, be restored periodically by clock signal.
6. The multi value logic (MVL) including binary systems as claimed in claim 1 comprising balanced and/or unbalanced system configuration.
7. The clock signal as claimed in claim 1 and 5 be inverted.

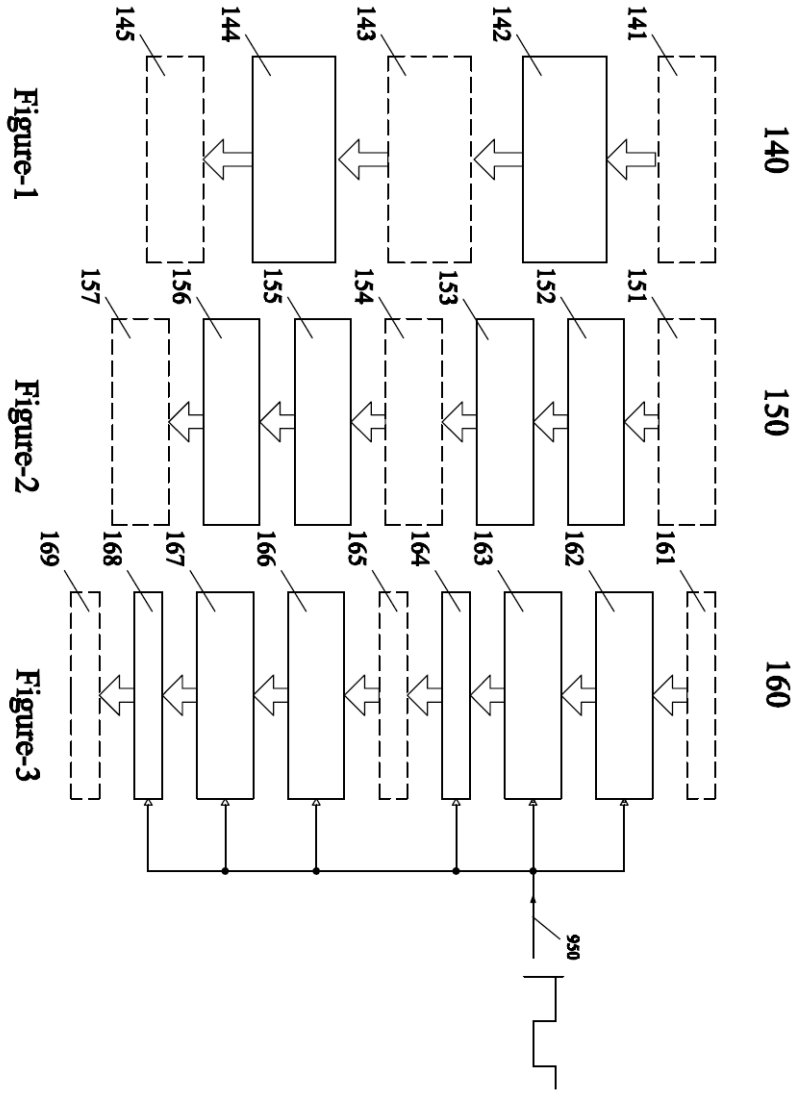

Figure-1

Figure-2

Figure-3

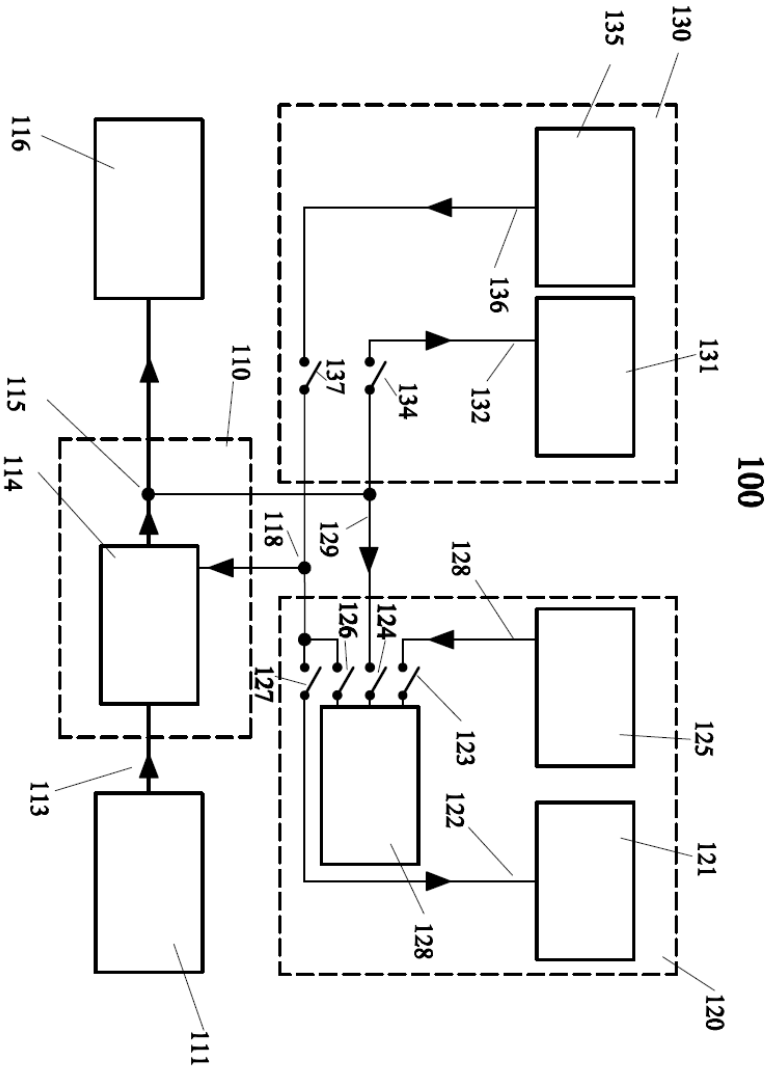
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Figure-4

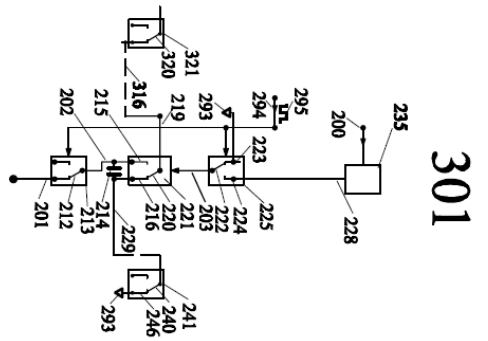

Figure-5

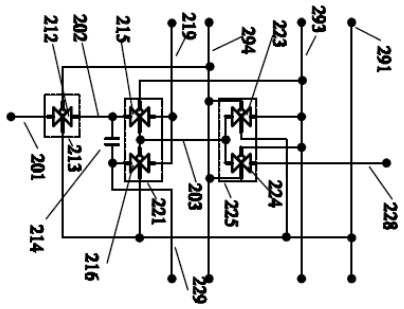

Figure-6

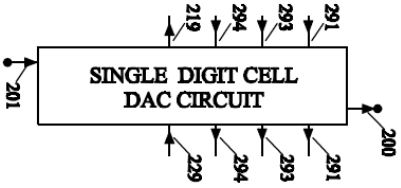

Figure-7

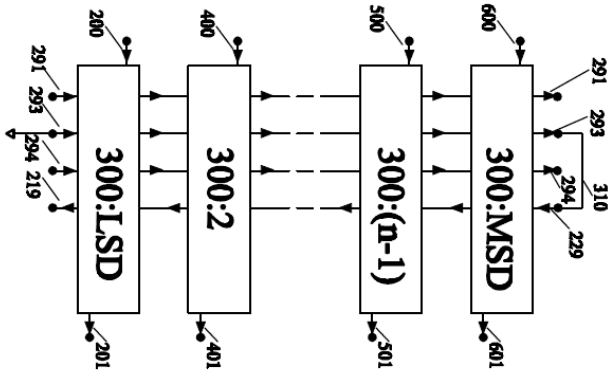

Figure-8

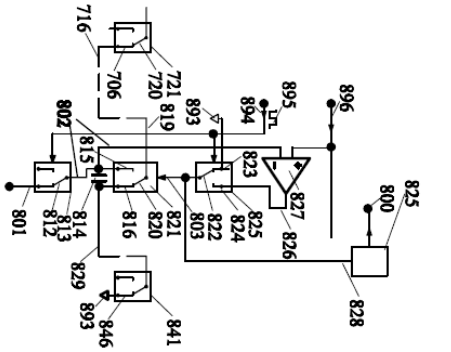

Figure- 9

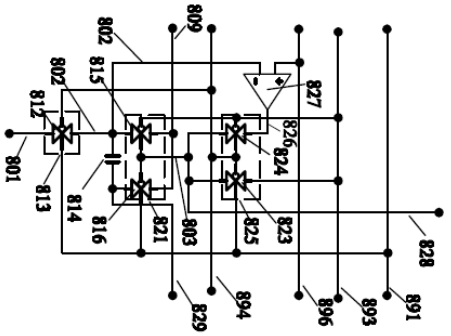

Figure-10

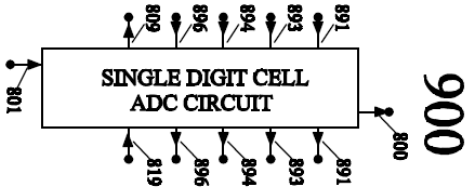

Figure-11

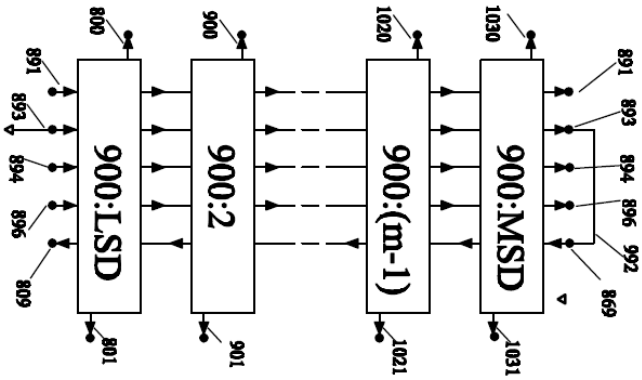

Figure- 12

ABSTRACT:-

Present invention generally relates to Analog to Digital Converter (ADC), Digital to Analog Converter (DAC) and digital to digital (DDC) for Multi Value Digital Logic including Binary Digit logic system and; particularly for Binary and Ternary Digital logic systems. The said DAC and ADC being simple and having low component count and comprises plurality of replicated digit cells rendering for easy implementation in modern VLSI technology and most importantly executes DAC, ADC and DDC operations in single cycle. Following invention is described in detail with the help of Figure 4 of sheet 2 shows the blocks of embodiments of the present invention and their interface.